

Round Rock 13.3" Schematics Document

Haswell ULT

2013-06-28

REV : SSI

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DY : None Installed

XDP: For CPU XDP Debug Port installed

PCH_XDP: For PCH XDP Debug Port installed

<Core Design>



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Title

Cover Page

Size
A3

Document Number

Round Rock 13.3" UMA

Rev
X00

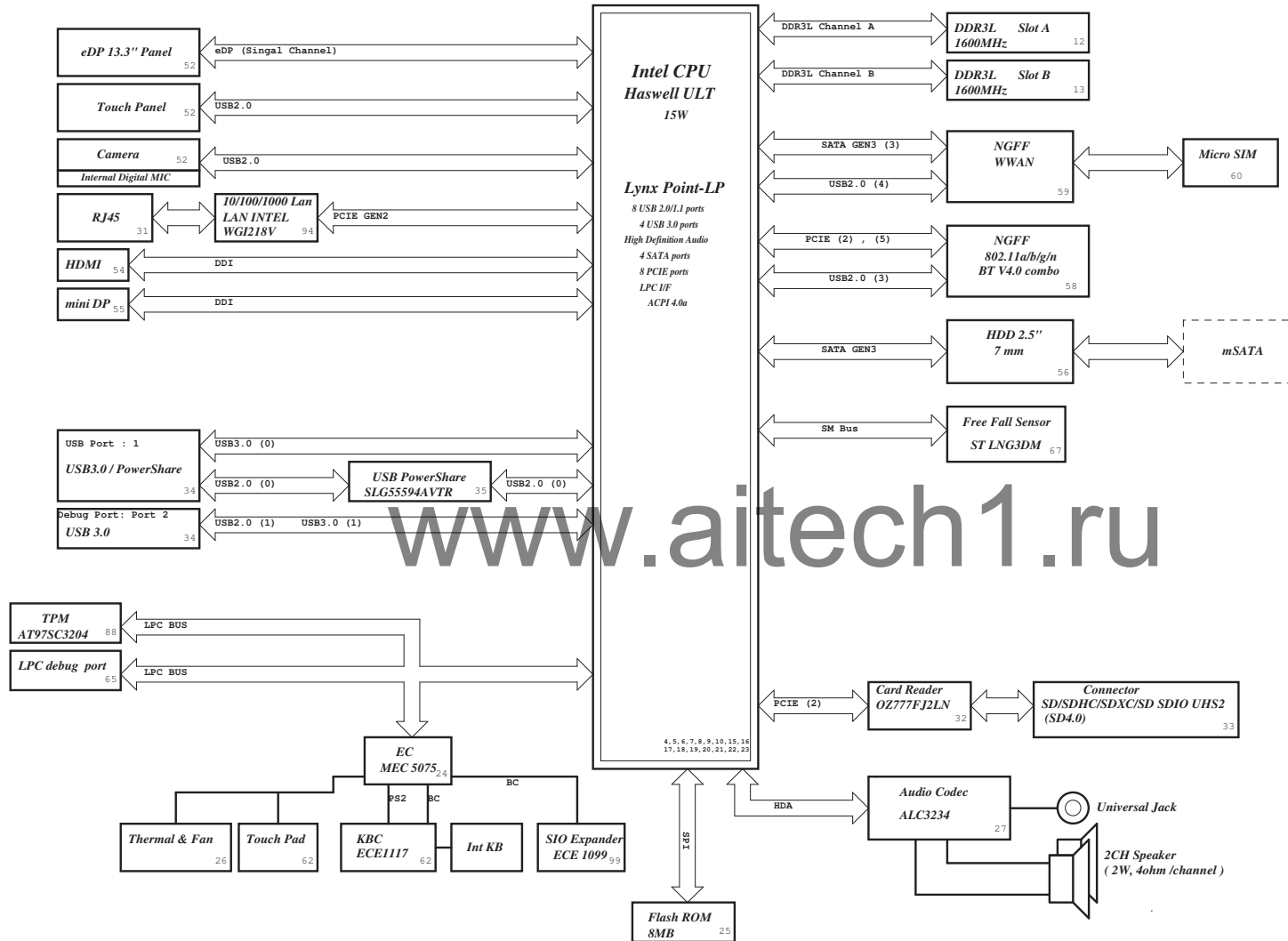
Date: Friday, June 28, 2013

Sheet 1 of 107

Round Rock 13.3" Block Diagram

Project code : 91.40A01.001
PCB P/N : 13229
Revision : X00

CHARGER BQ24715 44	
INPUTS	OUTPUTS
AD+ BT+	DCRATOUT
SYSTEM DC/DC TPS51275 45	
INPUTS	OUTPUTS
DCRATOUT	3.3V_AUX_S5 3.3V_S5 5V_S5
CPU DC/DC TPS51622 46-47	
INPUTS	OUTPUTS
DCRATOUT	VCC_CORE
SYSTEM DC/DC TPS51363 48	
INPUTS	OUTPUTS
DCRATOUT	ID05V_M
SYSTEM DC/DC TPS51363 & APL5338 49	
INPUTS	OUTPUTS
DCRATOUT	ID05V_S3 ID0675V_S0 DDR_VREF_S3
Load Switches 36	
INPUTS	OUTPUTS
5V_S3 3.3V_S3	5V_S0 3.3V_S0 3.3V_SS_PCH 3.3V_M 3.3V_LAN ID05V_MODPHY ID05V_S0
PCB LAYER(FR4-6 Layer)	
L1:Top L2:PW/GND L3:Signal L4:Signal L5:PW/GND	L6:Bottom



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Block Diagram	
File	Rev
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Date: Friday, June 28, 2013	Round Rock 13.3" UMA
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5

4

3

2

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Title

CPU (PCIE/DMI/FDI)

Size
A4

Document Number

Round Rock 13.3" UMA

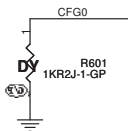
Rev
X00

Date: Friday, June 28, 2013

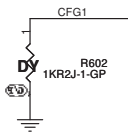
Sheet 3 of 107

SSID = CPU

EAR-STALL/NOT STALL RESET SEQUENCE AFTER PCU PLL IS LOCKE	
CFG0	0: Lane Reversed 1: (Default) Normal Operation; No stall

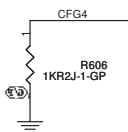


PCH/PCH LESS MODE SELECTION	
CFG1	0: Lane Reversed 1: (Default) Normal Operation

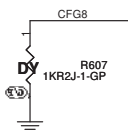


X01-20130204

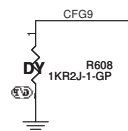
Display Port Presence Strap	
CFG4	1 : Disabled; No Physical Display Port attached to Embedded Display Port 0 : Enabled; An external Display Port device is connected to the Embedded Display Port



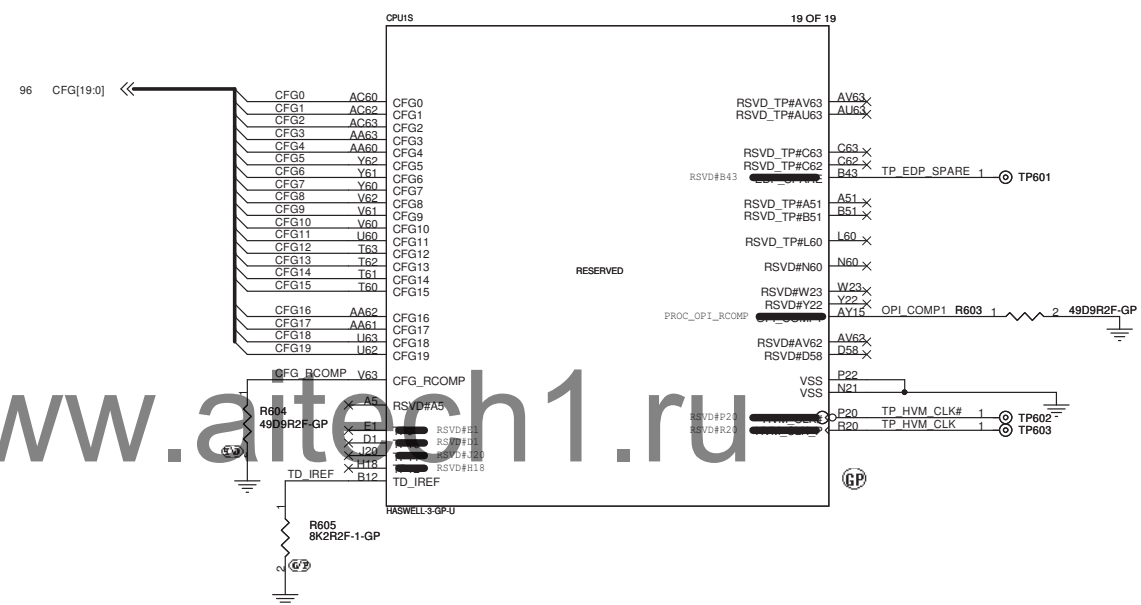
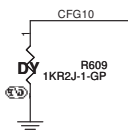
ALLOW THE USE OF NOA ON LOCKED UNITS	
CFG8	1: Enable(Default): Noa will be disable in locked units and enable in un-locked units 0: Enable Noa will be available pegrardless of the locking of the unit



NO SVID PROTOCOL CAPABLE VR CONNECTED	
CFG9	1: VRS support SVID protocol are present 0: No VR support SVID is present The chip will not generate (OR Respond to) SVID activity



SAFE MODE BOOT	
CFG10	1: POWER FEATURES ACTIVATED DURING RESET 0: POWER FEATURES (ESPECIALLY CLOCK GATINE ARE NOT ACTIVATED



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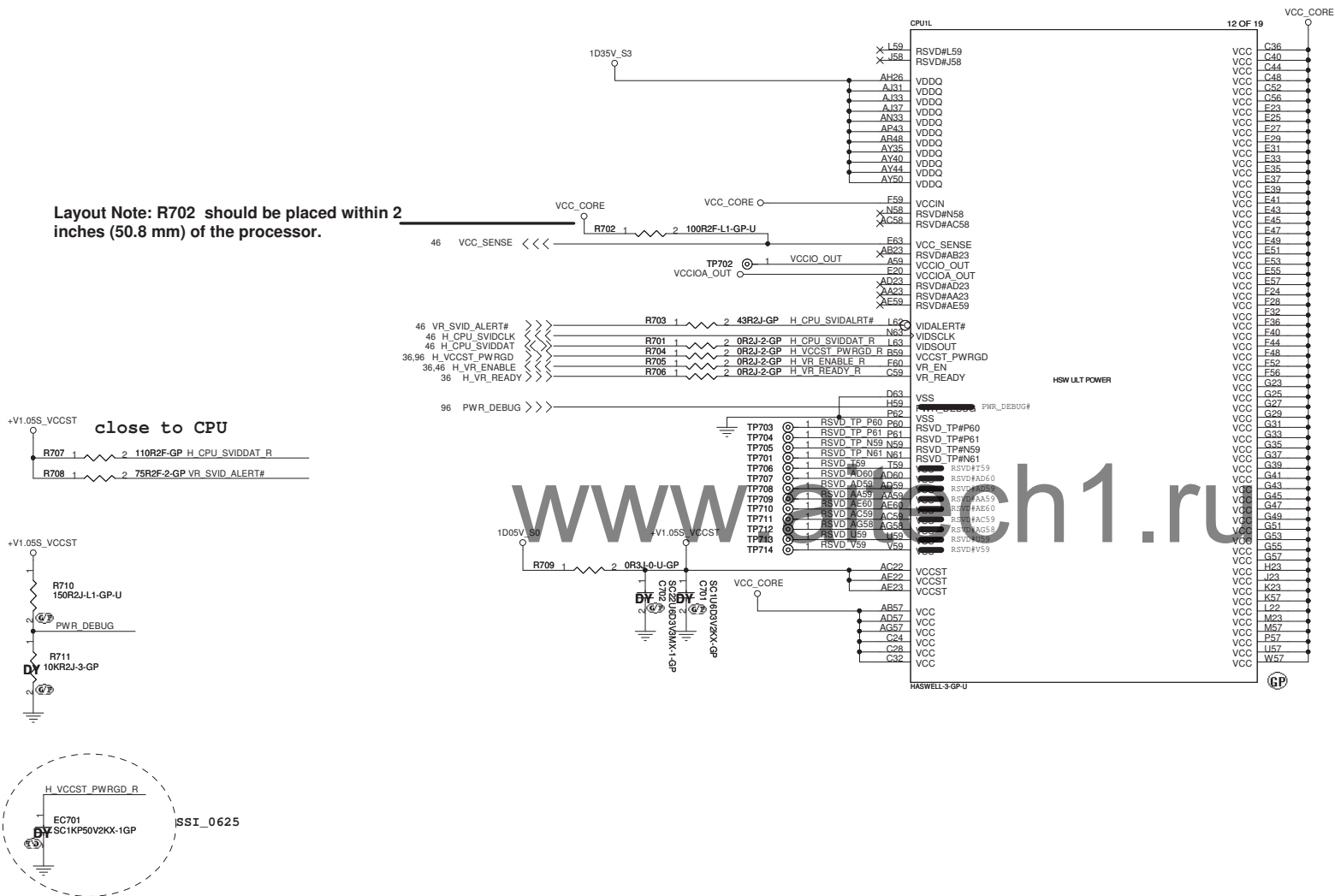
Title: **CPU (RESERVED)**

Size: A3 Document Number: **Round Rock 13.3" UMA** Rev: **X00**

Date: Friday, June 28, 2013 Sheet: 6 of 107

SSID = CPU

Layout Note: R702 should be placed within 2 inches (50.8 mm) of the processor.

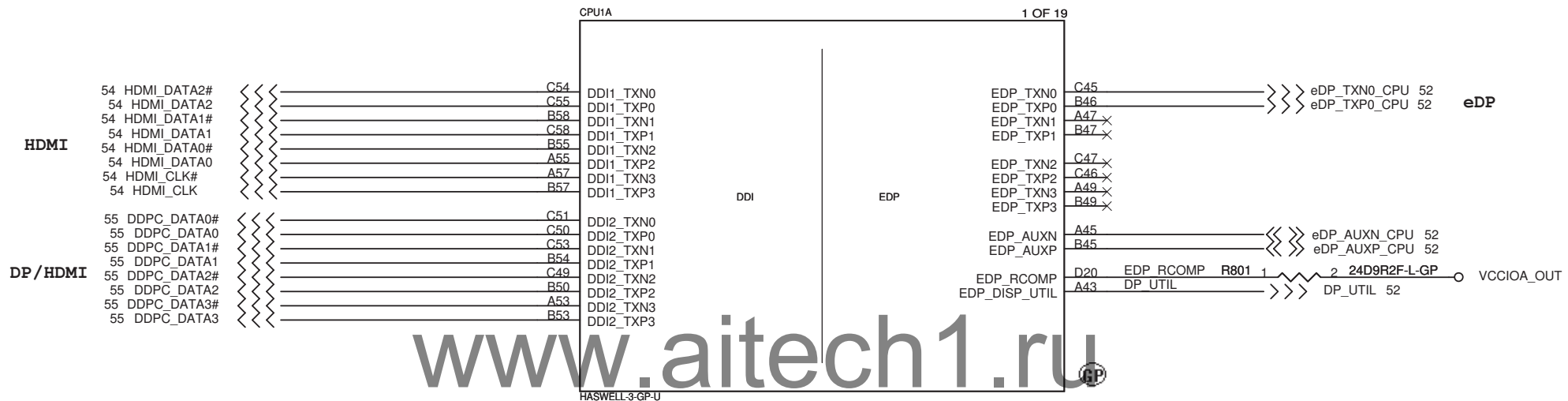


<Core Design>

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Title: **CPU (VCC CORE)**
Size: Custom Document Number: **Round Rock 13.3" UMA** Rev: **X00**
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SSID = CPU



DDI	HDMI	Display Port
DDI_TXN0	HDMI_DATA2_N	DP_LANE0_N
DDI_TXP0	HDMI_DATA2_P	DP_LANE0_P
DDI_TXN1	HDMI_DATA1_N	DP_LANE1_N
DDI_TXP1	HDMI_DATA1_P	DP_LANE1_P
DDI_TXN2	HDMI_DATA0_N	DP_LANE2_N
DDI_TXP2	HDMI_DATA0_P	DP_LANE2_P
DDI_TXN3	HDMI_CLK_N	DP_LANE3_N
DDI_TXP3	HDMI_CLK_P	DP_LANE3_P

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Title

CPU (DDI/EDP)

Size
A4

Document Number

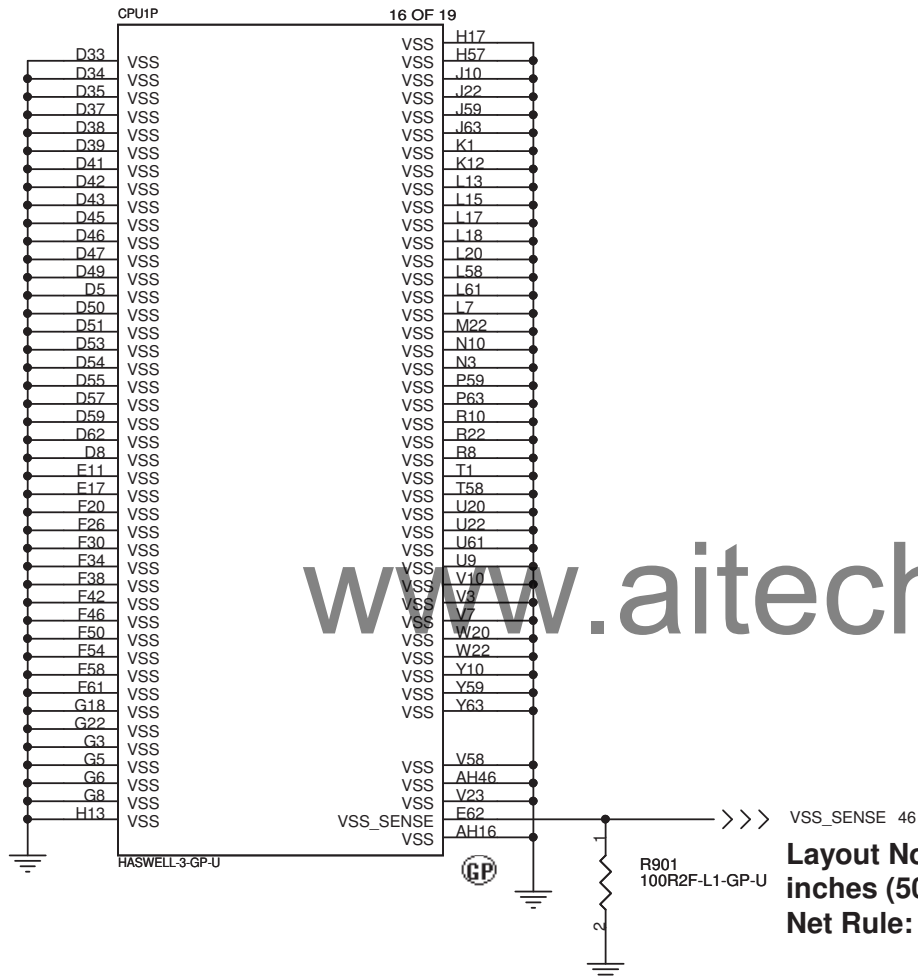
Round Rock 13.3" UMA

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X00

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SSID = CPU



Layout Note: R901 should be placed within 2 inches (50.8 mm) of the processor.
Net Rule: VCC_SENSE and VSS_SENSE differential signals

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Title

CPU (VSS)

Size
A4

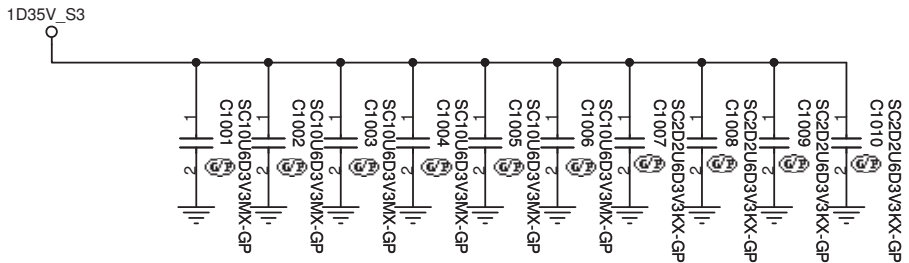
Document Number

Round Rock 13.3" UMA

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X00


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		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
CPU (Power CAP1)			
Size A4	Document Number		Rev X00
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Title

CPU (Power CAP2)

Size
A

Document Number

Round Rock 13.3" UMA

Rev

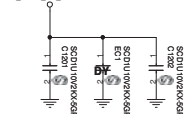
X00

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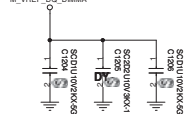
Layout Note:

M_VREF_CA_DIMMA



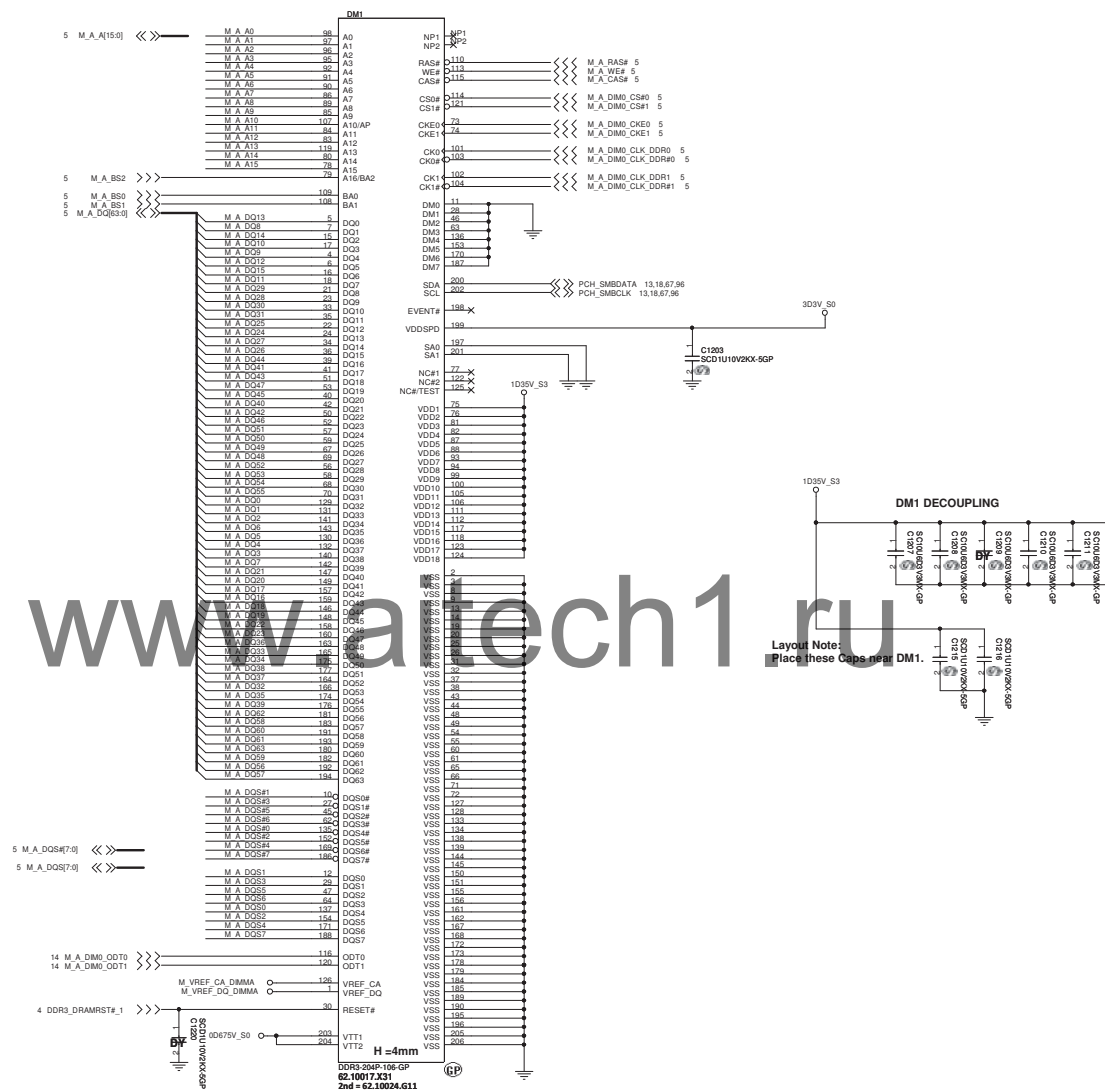
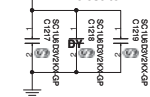
Layout Note:

M VREF DQ DIMMA



0D675V_S0

Place these caps close to VTT1 and VTT2.



Note:
If SA0_DIM0 = 0, SA1_DIM0 = 0
SO-DIMMA SPD Address is 0xA0
SO-DIMMA TS Address is 0x30

If SA0_DIM0 = 1, SA1_DIM0 = 0
SO-DIMMA SPD Address is 0xA2
SO-DIMMA TS Address is 0x32

Layout Note:
Place these Caps near DM1

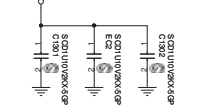
<Core Design>



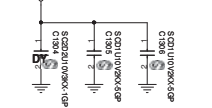
Title			
DDR3L-SODIMM1			
Size A2	Document Number	Round Rock 13.3" UMA	Rev X0
Date: Friday, June 28, 2013	Sheet	12	of 107

SSID = MEMORY

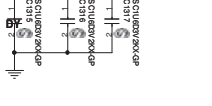
Layout Note:
Place these caps close to VREF_CA
M_VREF_CA_DIMMB



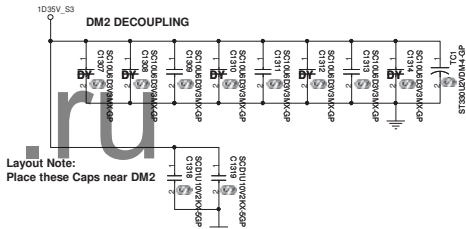
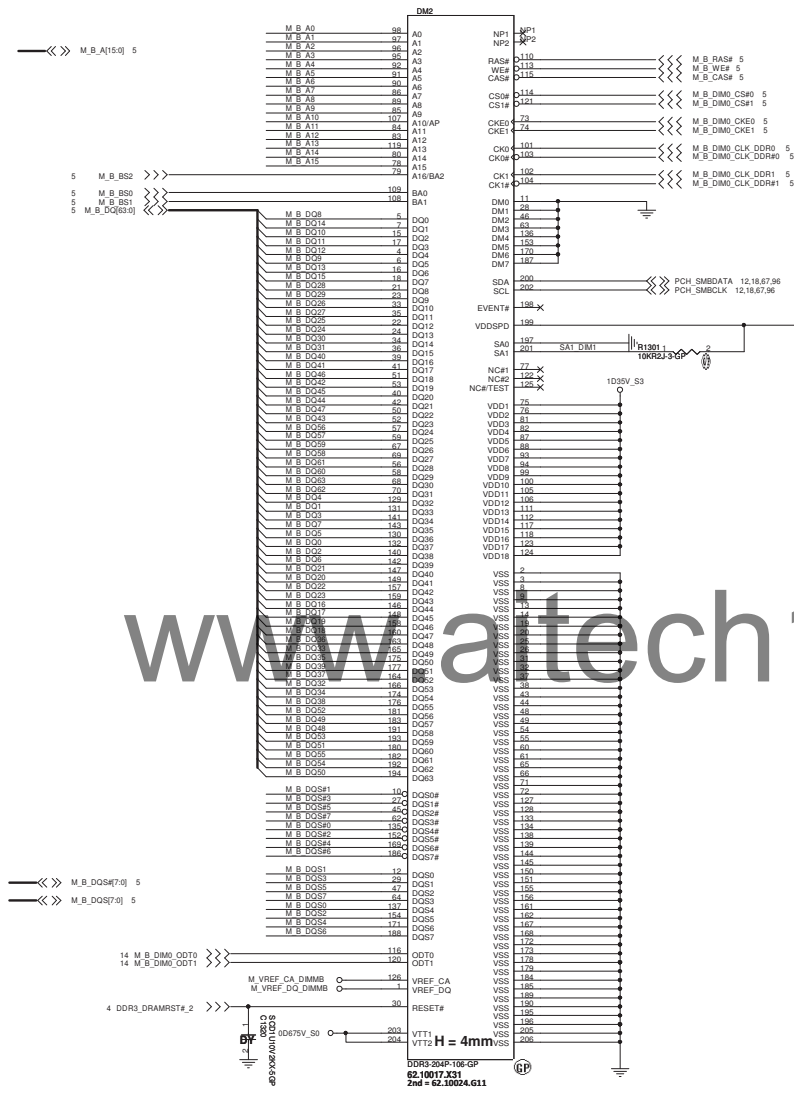
Layout Note:
Place these caps close to VREF_DQ
M_VREF_DQ_DIMMB



Place these caps
close to VTT1 and VTT2.



DQS1	DQ0	M_B_DQ8
	DQ1	M_B_DQ14
	DQ2	M_B_DQ10
	DQ3	M_B_DQ11
	DQ4	M_B_DQ12
	DQ5	M_B_DQ9
	DQ6	M_B_DQ13
	DQ7	M_B_DQ15
DQS3	DQ8	M_B_DQ28
	DQ9	M_B_DQ29
	DQ10	M_B_DQ26
	DQ11	M_B_DQ27
	DQ12	M_B_DQ25
	DQ13	M_B_DQ24
	DQ14	M_B_DQ30
	DQ15	M_B_DQ31
DQS5	DQ16	M_A_DQ40
	DQ17	M_A_DQ41
	DQ18	M_A_DQ46
	DQ19	M_A_DQ42
	DQ20	M_A_DQ45
	DQ21	M_A_DQ44
	DQ22	M_A_DQ47
	DQ23	M_A_DQ43
DQS7	DQ24	M_A_DQ56
	DQ25	M_A_DQ57
	DQ26	M_A_DQ59
	DQ27	M_A_DQ58
	DQ28	M_A_DQ61
	DQ29	M_A_DQ60
	DQ30	M_A_DQ63
	DQ31	M_A_DQ62
DQS0	DQ32	M_A_DQ4
	DQ33	M_A_DQ1
	DQ34	M_A_DQ3
	DQ35	M_A_DQ7
	DQ36	M_A_DQ5
	DQ37	M_A_DQ0
	DQ38	M_A_DQ2
	DQ39	M_A_DQ6
DQS2	DQ40	M_A_DQ21
	DQ41	M_A_DQ20
	DQ42	M_A_DQ22
	DQ43	M_A_DQ23
	DQ44	M_A_DQ16
	DQ45	M_A_DQ17
	DQ46	M_A_DQ19
	DQ47	M_A_DQ18
DQS4	DQ48	M_A_DQ36
	DQ49	M_A_DQ33
	DQ50	M_A_DQ35
	DQ51	M_A_DQ37
	DQ52	M_A_DQ39
	DQ53	M_A_DQ32
	DQ54	M_A_DQ34
	DQ55	M_A_DQ38
DQS6	DQ56	M_A_DQ52
	DQ57	M_A_DQ49
	DQ58	M_A_DQ48
	DQ59	M_A_DQ51
	DQ60	M_A_DQ53
	DQ61	M_A_DQ55
	DQ62	M_A_DQ54
	DQ63	M_A_DQ50

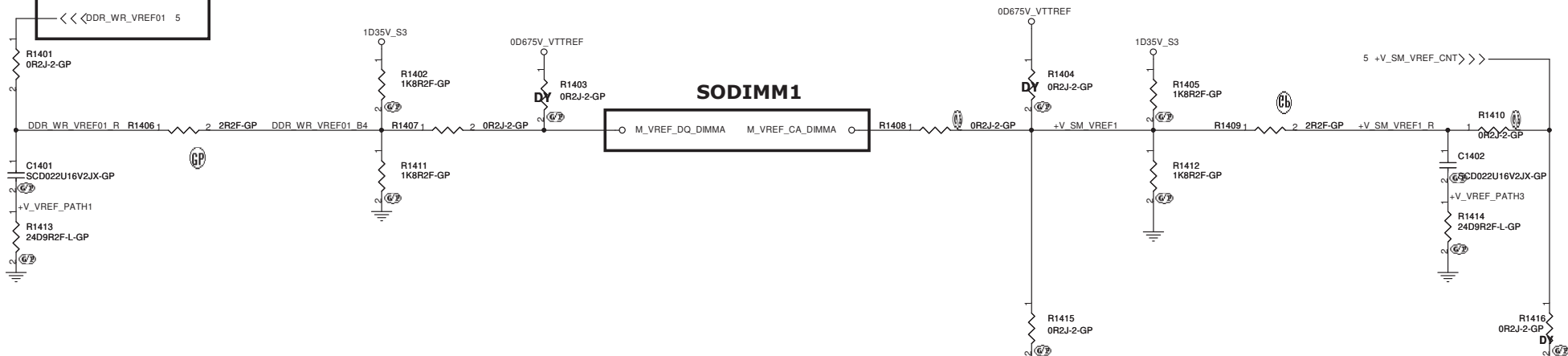


Layout Note:
Place these Caps near DM2

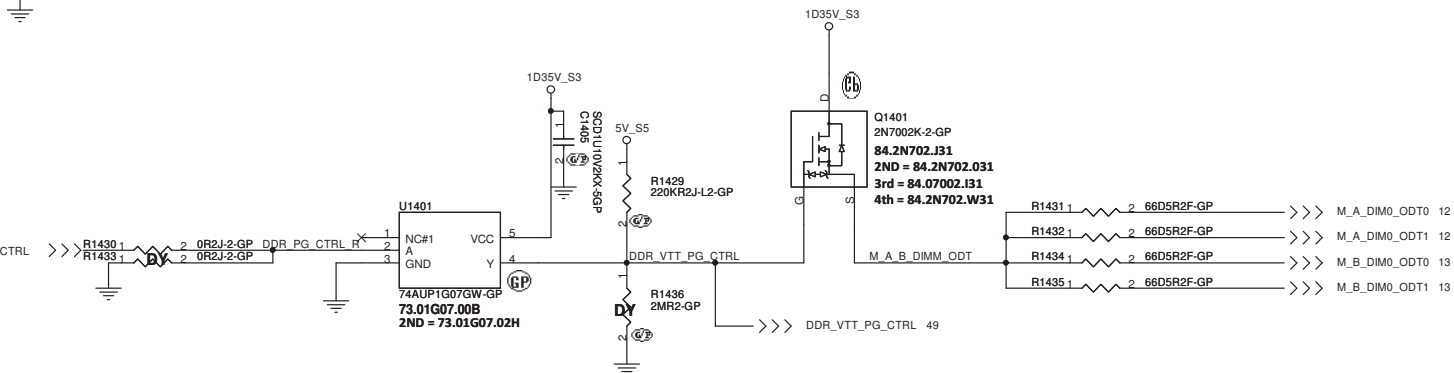
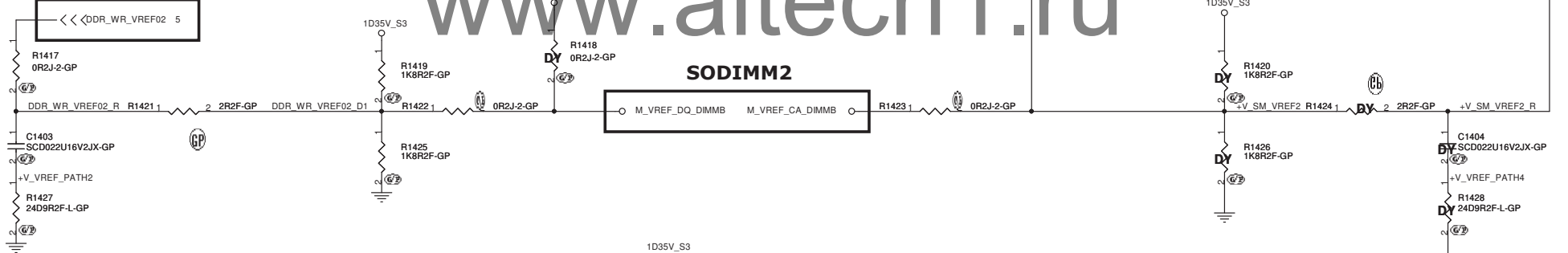
Note:
SO-DIMMB SPD Address is 0xA4
SO-DIMMB TS Address is 0x34
SO-DIMMB is placed farther from
the Processor than SO-DIMMA

SSID = MEMORY VREF circuit -M1 (Voltage Driver Network) & M3 (Driven by Processor) Implementation

SA_DIMM_VREFDQ Driven by process (PIN#AR51)



SB_DIMM_VREFDQ Driven by process (PIN#AP51)



<Core Design>

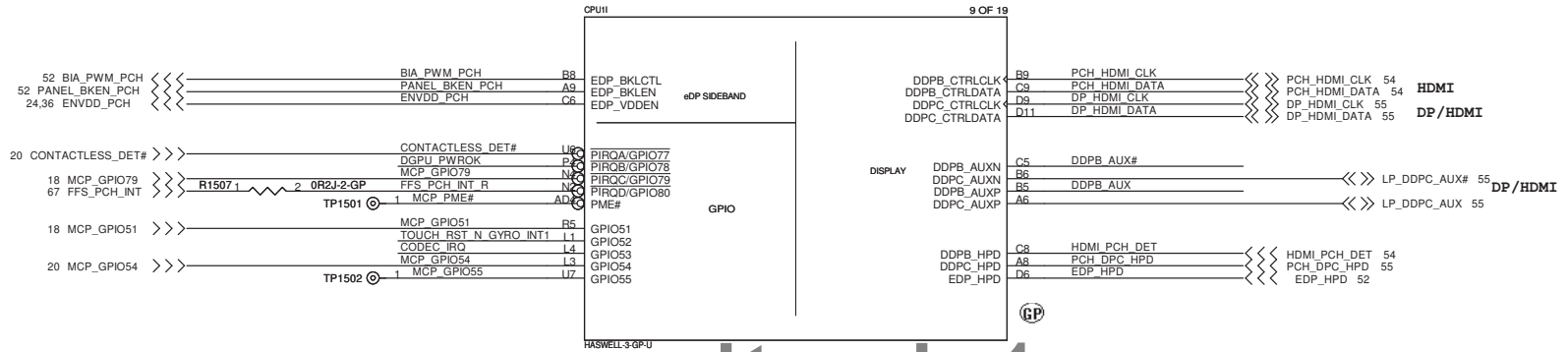
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Title: **M1 & M3 Implementation**

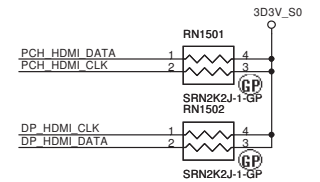
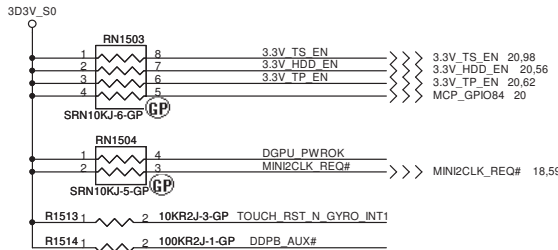
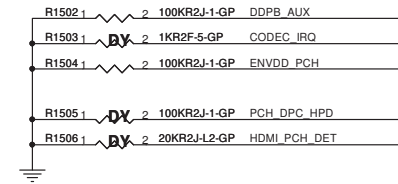
Size: A3 Document Number: **Round Rock 13.3" UMA** Rev: X00

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MCP_GPIO79 R1508 1 2 0R2J-2-GP FFS_PCH_INT



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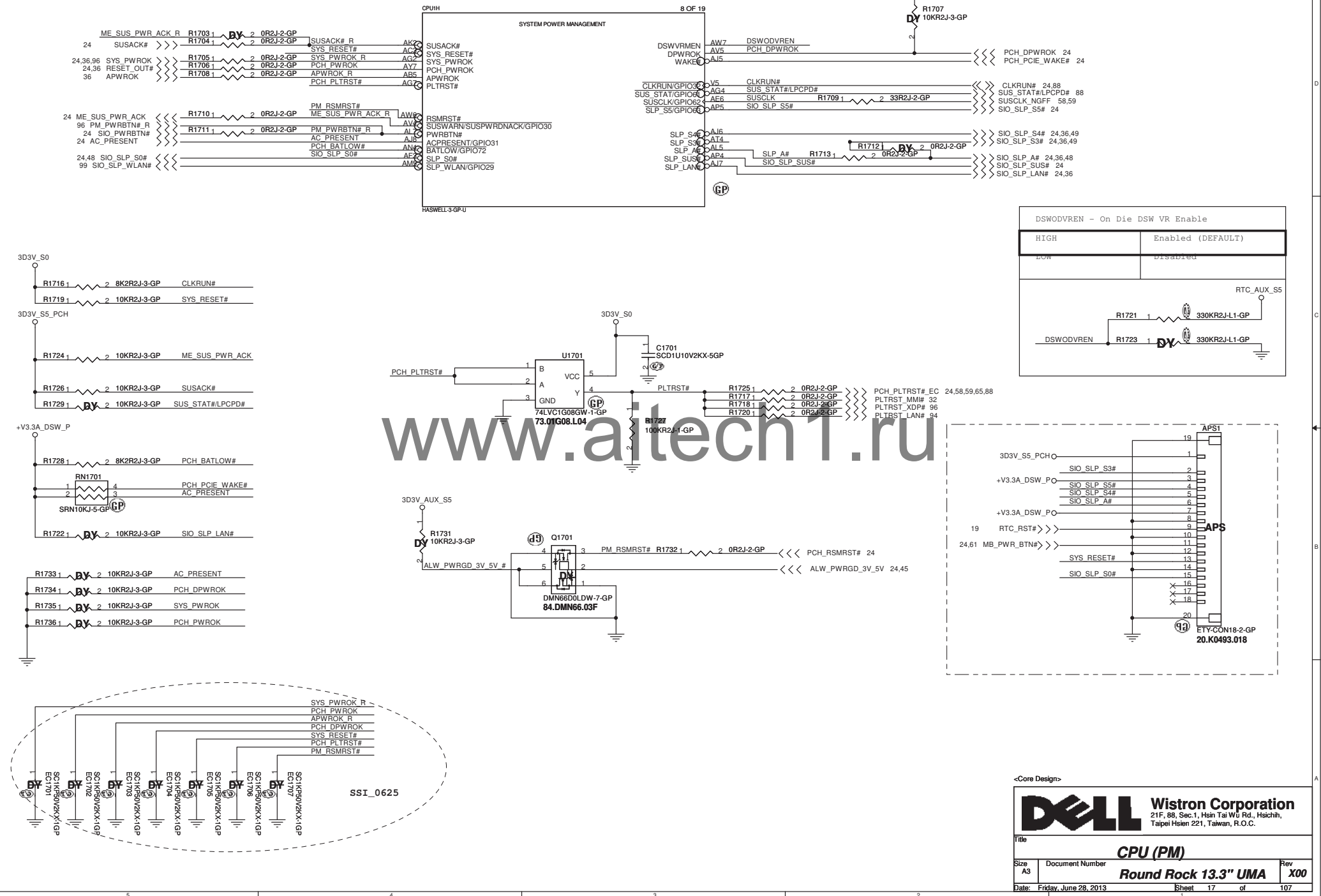


<Core Design>

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		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title CPU (DDI/PCI)			
Size A3	Document Number Round Rock 13.3" UMA	Rev X00	
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SSID = PCH

NOTE:
PWRBTN# Integrated Pull-Up.



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Title: **CPU (PM)**

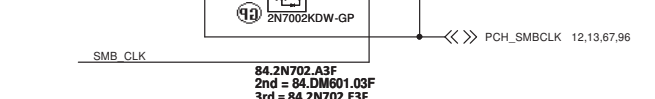
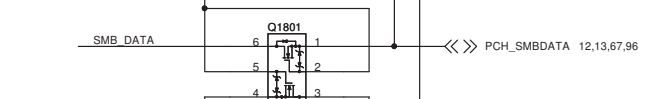
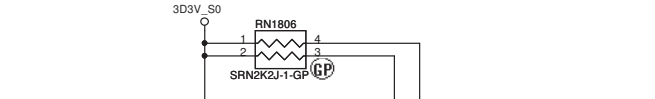
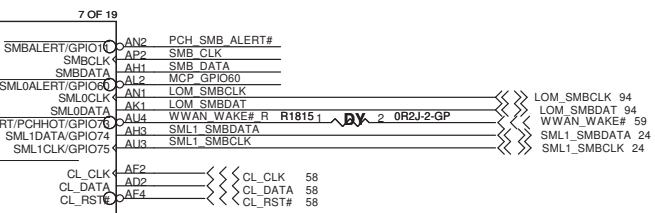
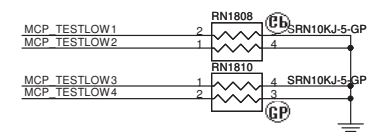
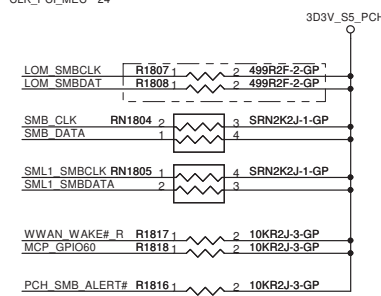
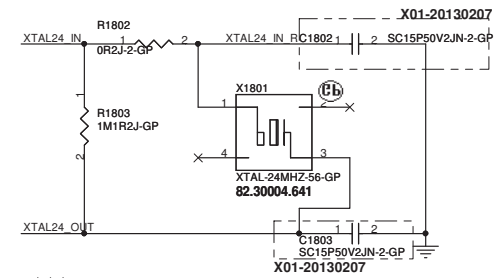
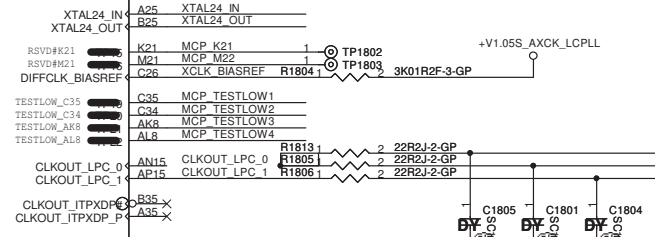
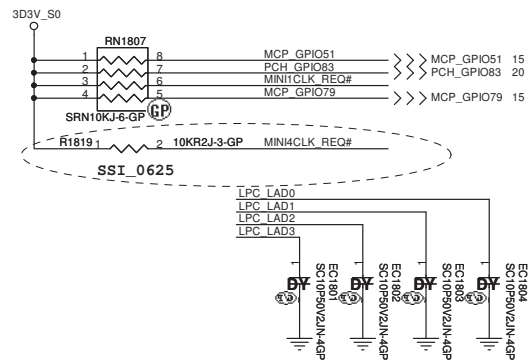
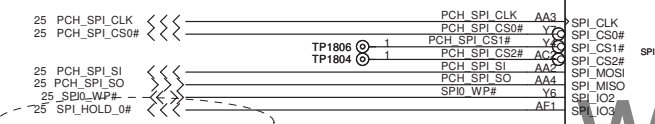
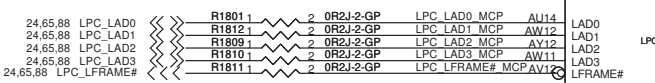
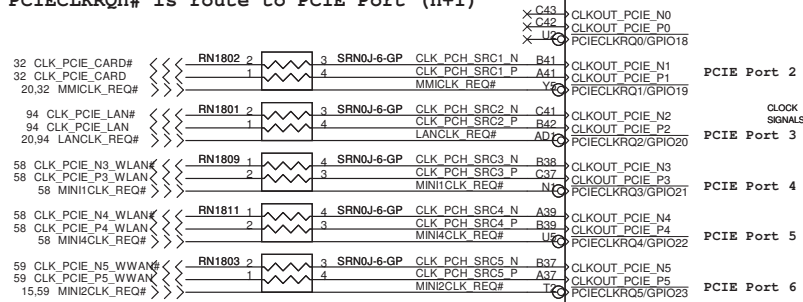
Size: A3 Document Number: **Round Rock 13.3" UMA** Rev: **X00**

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SSID = PCH

PCIECLKRQ1# and PCIECLKRQ2#
Support S0 power only

PCIECLKRQn# is route to PCIE Port (n+1)



The diagram is a schematic for the CPU (RTC/SATA/HDA/JTAG) section of a Dell W1300 laptop. It shows the CPU (5 OF 19) connected to various components including RTC, AUDIO, SATA, JTAG, and storage devices (HDD, WWAN). The diagram includes a Flash Descriptor Security Override table and a core design section with Dell and Wistron Corporation logos.

Flash Descriptor Security Override

Flash Descriptor Security Override	
HDA_SDOOUT	Low = Default High = Enable

Core Design

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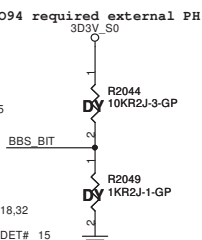
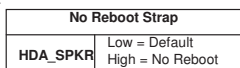
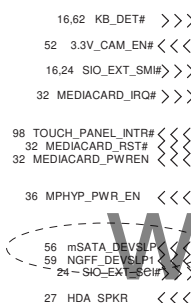
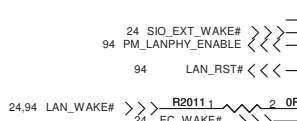
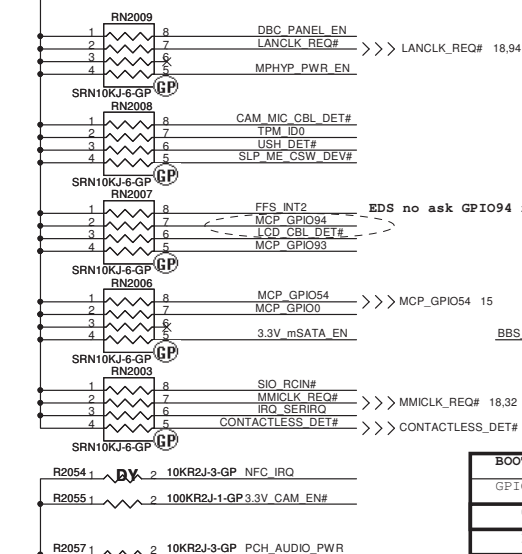
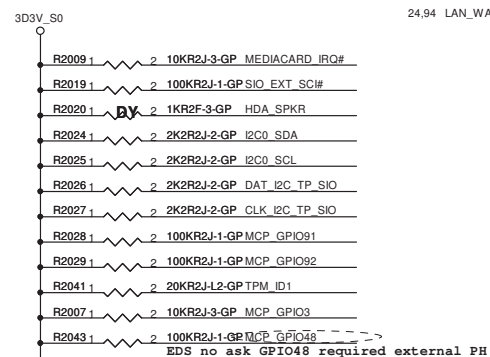
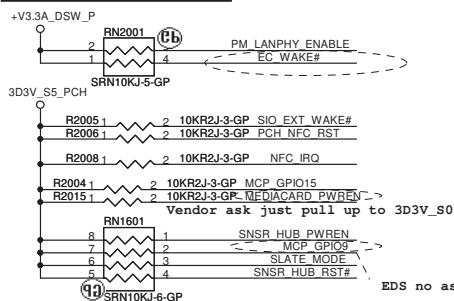
File
CPU (RTC/SATA/HDA/JTAG)

Size A3 **Document Number** **Round Rock 13.3" UMA** **Rev** X00

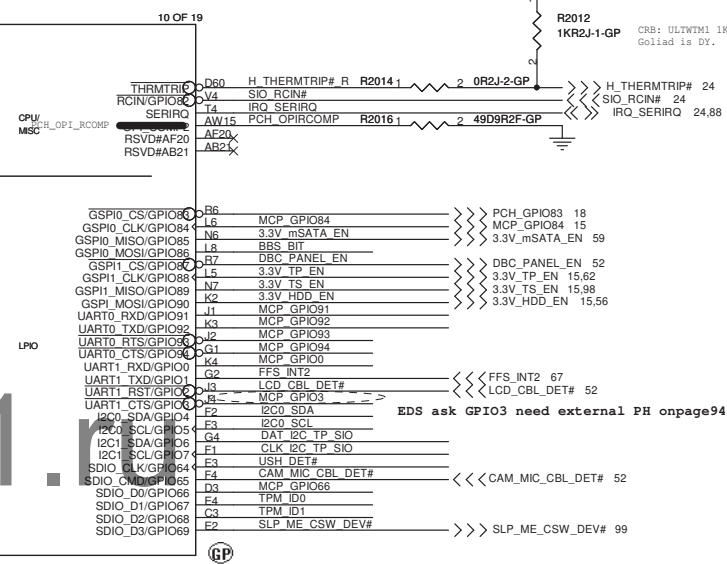
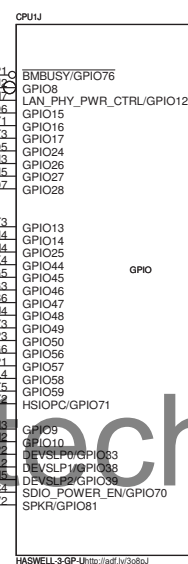
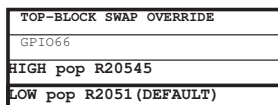
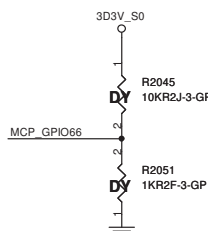
Date: Friday, June 28, 2013 **Sheet** 19 **of** 107

<Core Design>			
		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
<i>CPU (RTC/SATA/HDA/JTAG)</i>			
Size A3	Document Number	<i>Round Rock 13.3" UMA</i>	
Date: Friday, June 28, 2013	Sheet	19	of 107

SSID = PCH



BOOT BIOS Strap	
GPI086	BOOT BIOS Location
0	SPI(Default)
1	LPC



<http://adf.ly/3o8pJ>

<Core Design>



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Title

CPU (GPIO/CPU)

Size

Document Number

Round Rock 13.3" UMA

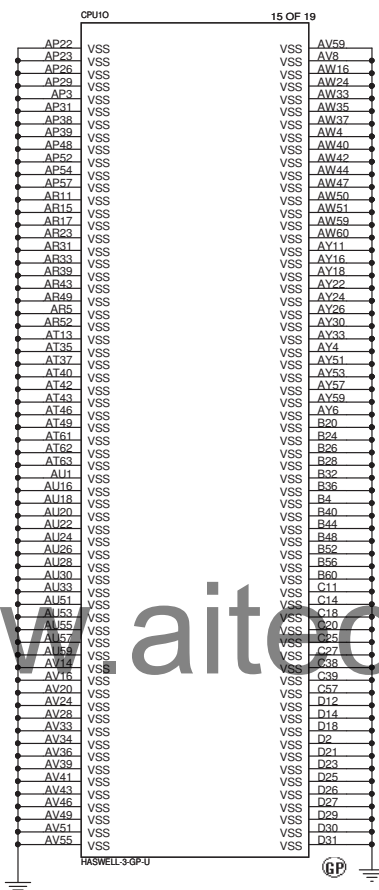
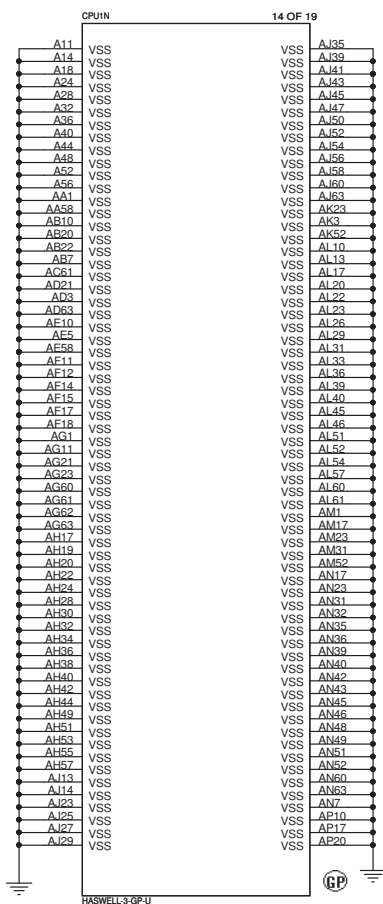
Date _____

Friday, June 28, 2013

Sheet 20 of 107

Rev

SSID = PCH



<Core Design>



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Title

CPU (VSS)

Size

A3 Document Number

Round Rock 13.3" UMA

Rev

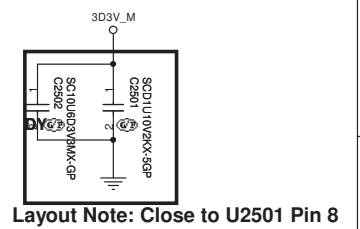
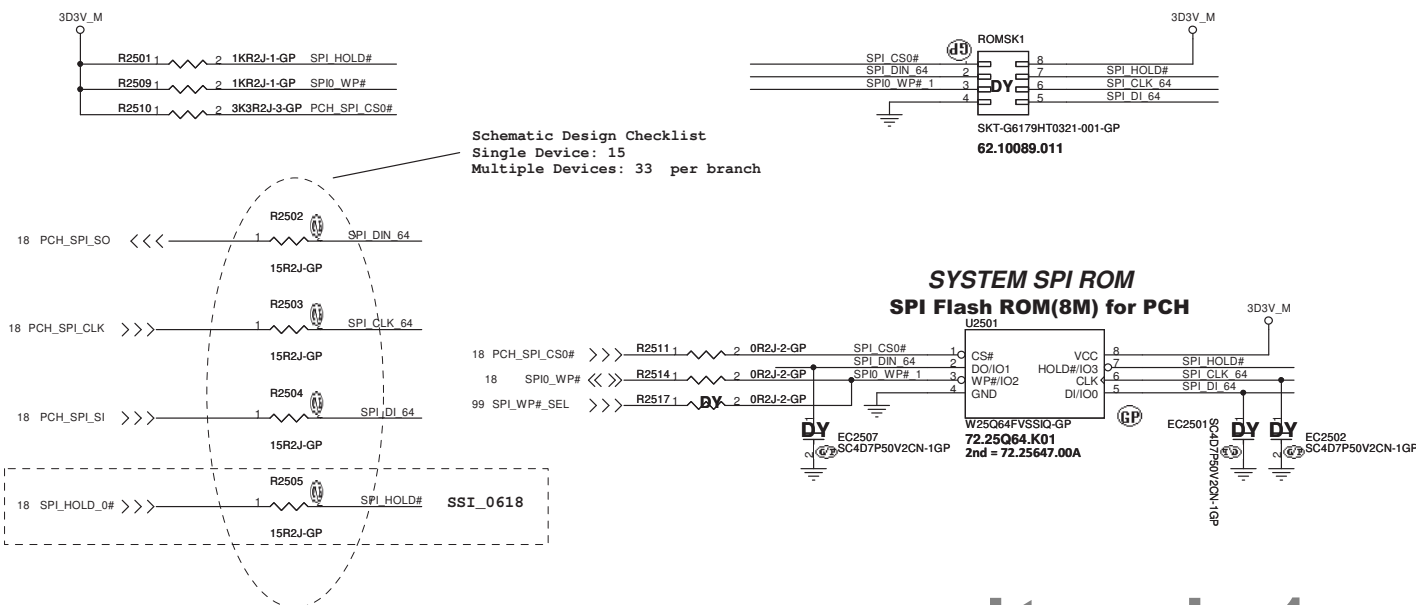
X00

Date: Friday, June 28, 2013

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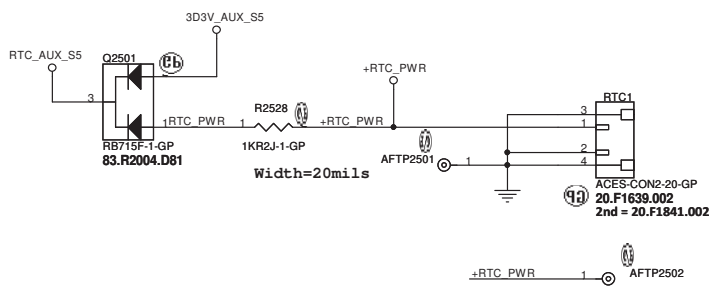
SSID = Flash.ROM

SPI ROM Equal length need to less than 500mil



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SSID = RTC



<Core Design>

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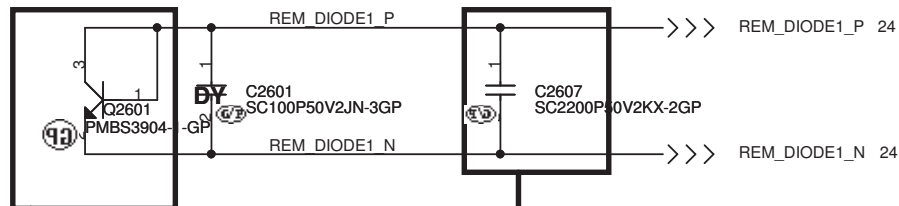
Title **Flash/RTC**

Size A3 Document Number **Round Rock 13.3" UMAX00** Rev

Date: Friday, June 28, 2013 Sheet 25 of 107

SSID = Thermal

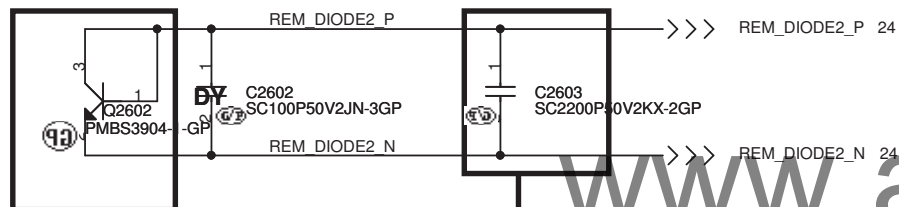
84.03904.L06
2ND = 84.03904.P11



Layout Note: Place to CPU

Both DXN and DXP routing 10 mil trace width and 10 mil spacing.

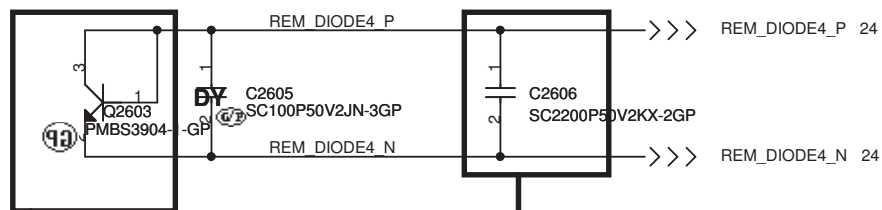
84.03904.L06
2ND = 84.03904.P11



Layout Note: Place to DIMM

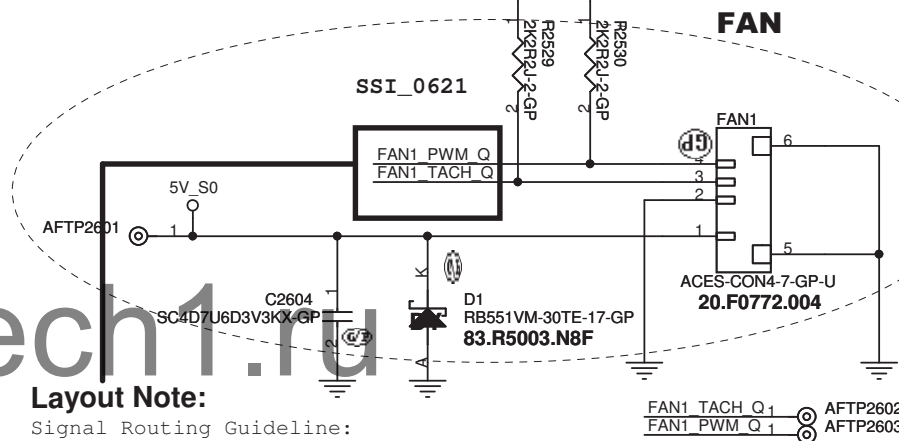
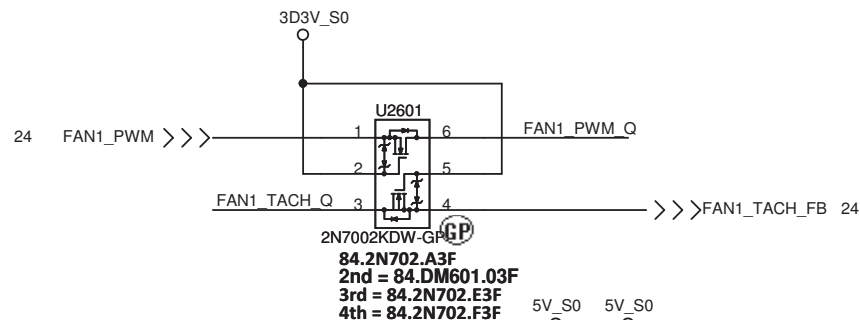
Both DXN and DXP routing 10 mil trace width and 10 mil spacing.

84.03904.L06
2ND = 84.03904.P11



Layout Note: Place to V.R

Both DXN and DXP routing 10 mil trace width and 10 mil spacing.



Layout Note:

Signal Routing Guideline:
Trace width = 15mil

<Core Design>



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Title

Thermal/Fan

Size
A4

Document Number

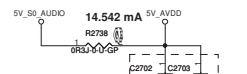
Round Rock 13.3" UMA

Rev
X00

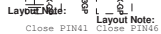
Date: Friday, June 28, 2013

Sheet 26 of 107

SSID = AUDIO



Place close to Pin 26

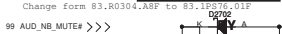


```

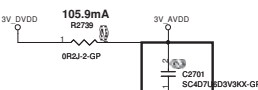
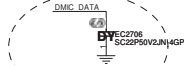
..... trace width=30
.....

```

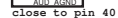
Digital



DMIC: > 5mil and keep out the analog signal
close to pin 3



close to pin 36



Place close to Pin 13. —



X01 1121 To slove background noise



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<Core Design>



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Title

Reserved

Size
A

Document Number

Round Rock 13.3" UMA

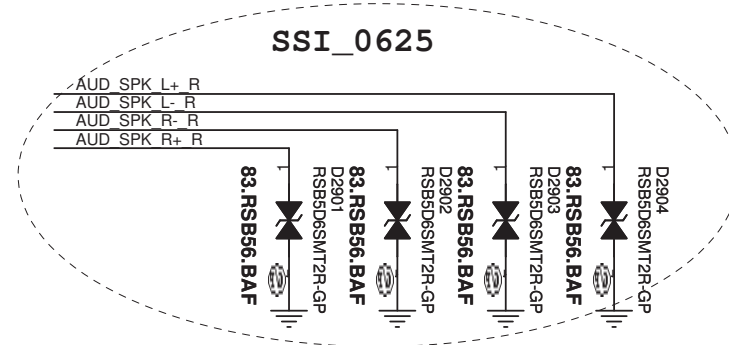
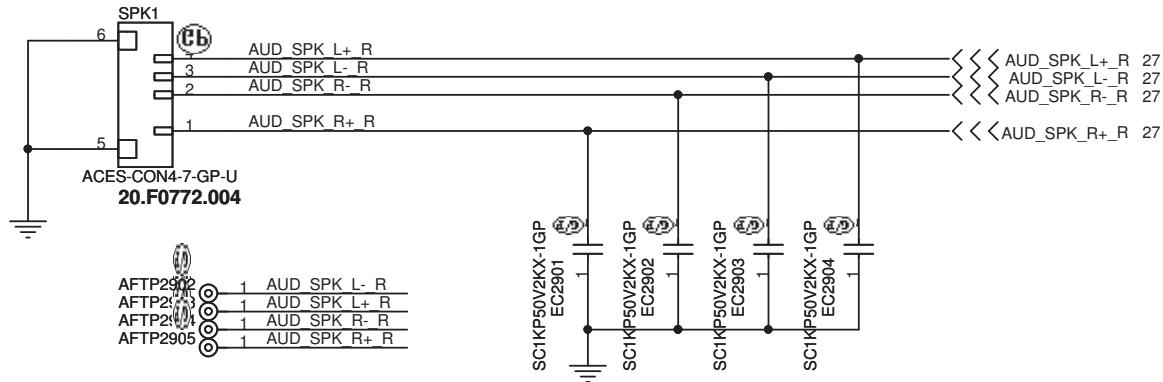
Rev
X00

Date: Friday, June 28, 2013

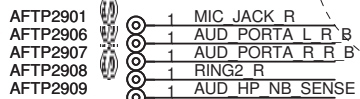
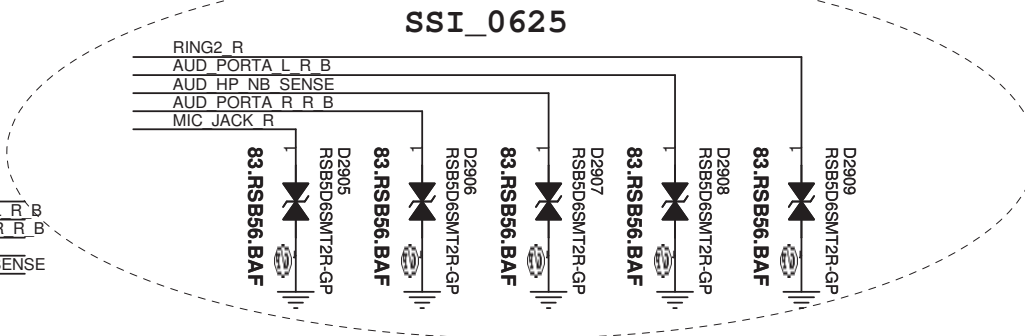
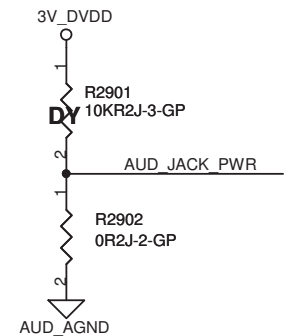
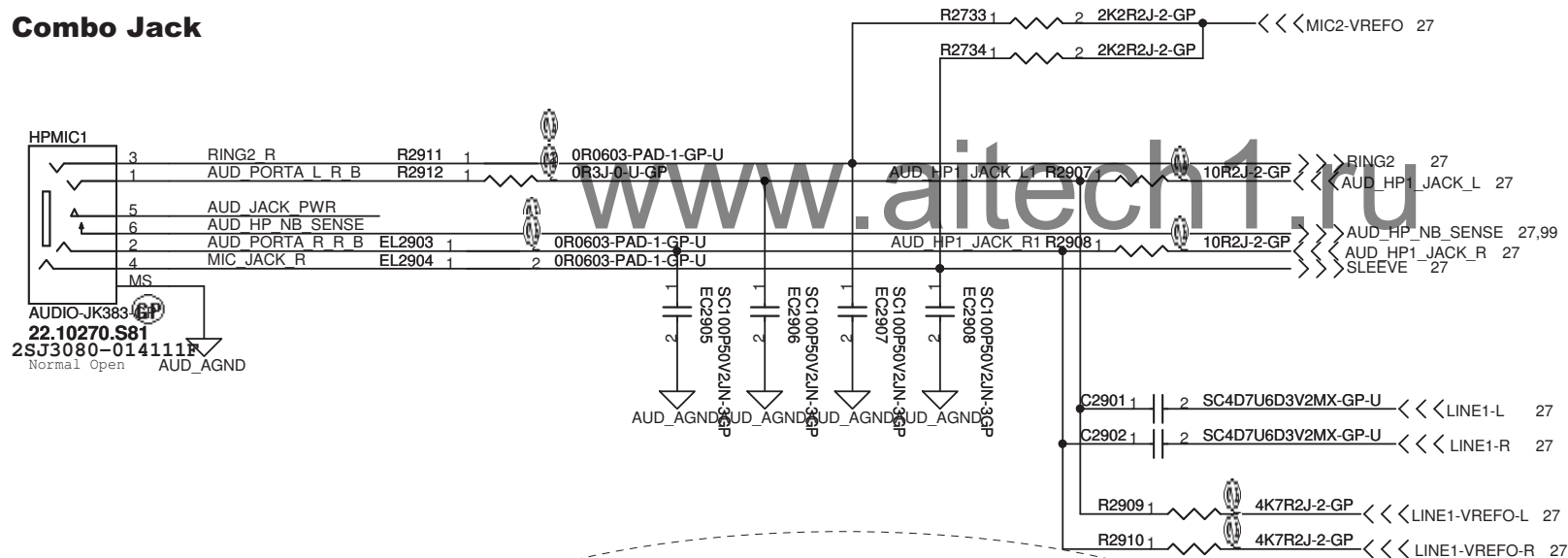
Sheet 28 of 107

SSID = AUDIO

Speaker 2W/ch



Combo Jack



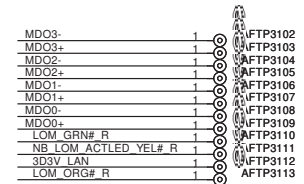
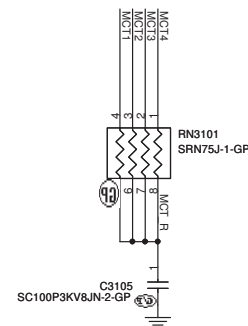
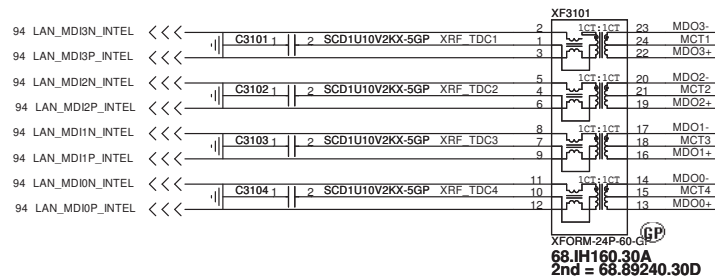
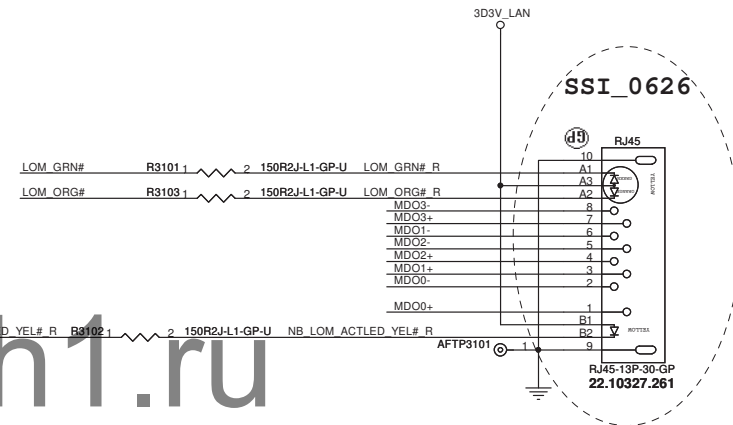
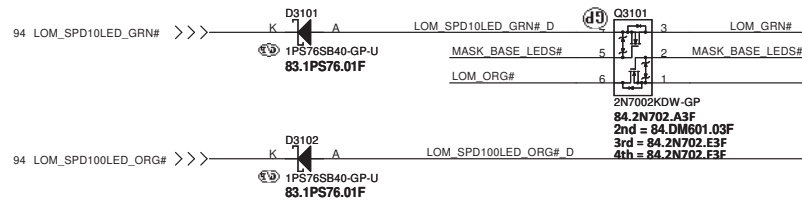
<Core Design>



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Title		
Speaker/HPMIC CONN		
Size	Document Number	Rev
A4		X00
Date:	Friday, June 28, 2013	Sheet 29 of 107

SSID = LOM



<Core Design>

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Title **RJ45/Transformer**

Size A3 Document Number **Round Rock 13.3" UM100** Rev

Date: Friday, June 28, 2013 Sheet 31 of 107

Bead Spec update to 100MHZ/600 ohm/600mA


Layout Note:

add one more pull down 1Mohm resistor on SD_CD# for the OZ777FJ2LN-A.
For the OZ777FJ2LN-B, you can remove these 1Mohm resistor and 0.1uF capacitor.

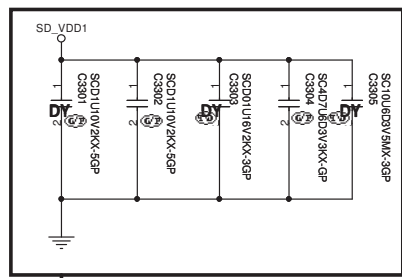
SD_D0P	SD_D1P	33	For UHS-II
SD_D1N	SD_D1N	33	
SD_D0N	SD_D0N	33	
SD_D0P	SD_D0P	33	

Layout Note: Differential impedance of 100 Ohm

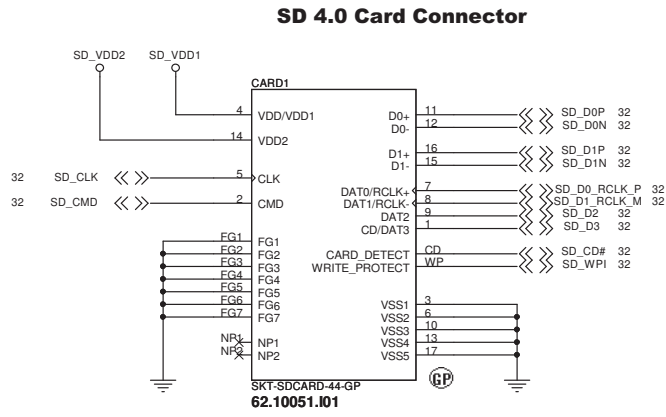
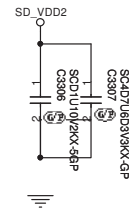
IO0_LDSEL:
High means select internal LDO for main area core power.
Low means select external LDO for main area core power.

<Core Design>			
		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
		Card Reader	
Size A3	Document Number	Round Rock 13.3" UMA	
Date:	Friday, June 28, 2013	Sheet	32 of 107

SSID =Card Reader

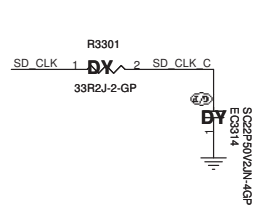
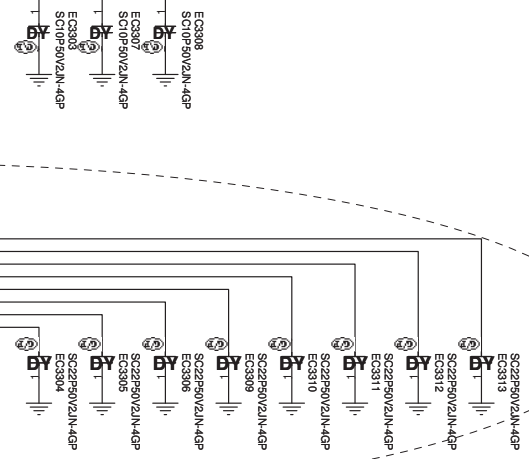


Layout Note:Close to Card Reader CONN



SD_CD#	1	AFTP3301
SD_D3	1	AFTP3302
SD_CLK	1	AFTP3303
SD_CMD	1	AFTP3304
SD_D0_RCLK_P	1	AFTP3305
SD_D1_RCLK_M	1	AFTP3306
SD_D2	1	AFTP3307
SD_WPI	1	AFTP3308
SD_VDD1	1	AFTP3309
SD_D0P	1	AFTP3311
SD_D0N	1	AFTP3312
SD_D1P	1	AFTP3313
SD_D1N	1	AFTP3310

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SSI_0625

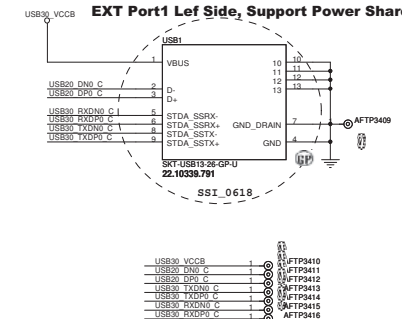
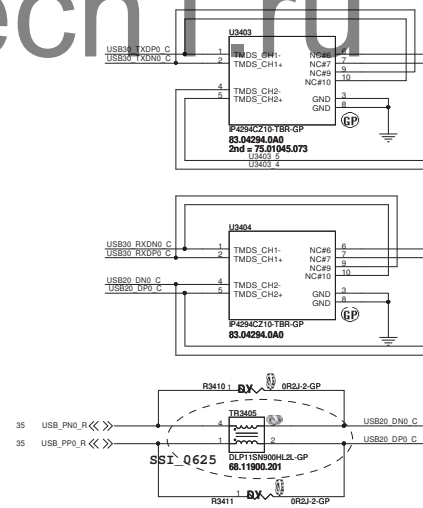
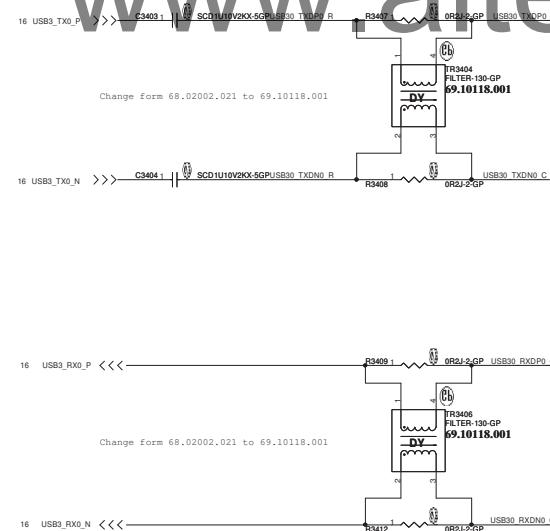
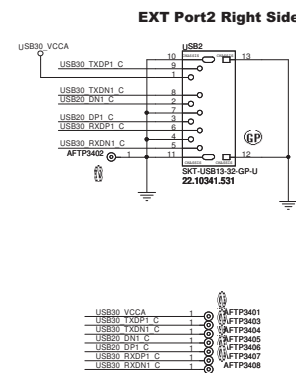
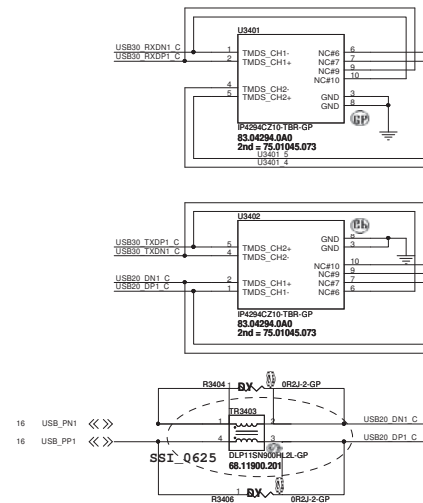
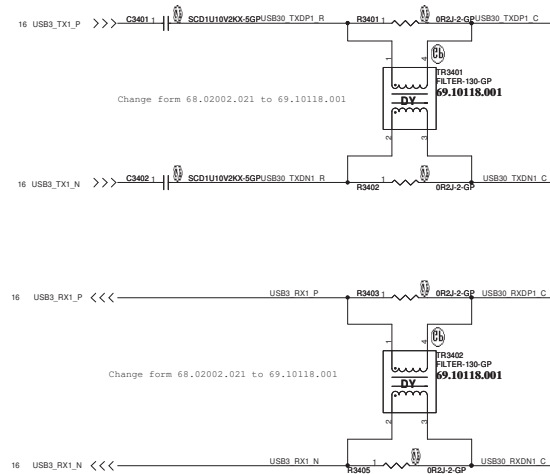
<Core Design>

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Title **Card Reader CONN**

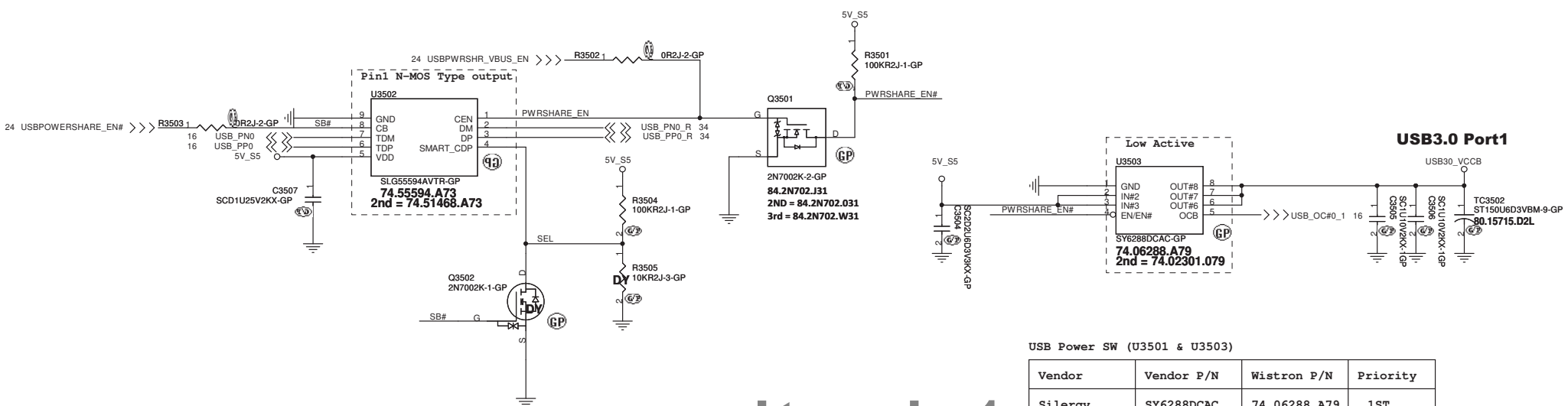
Size A3	Document Number Round Rock 13.3" UMA	Rev X00
Date: Friday, June 28, 2013	Sheet 33 of 107	

SSID = USB



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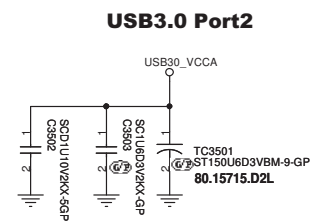
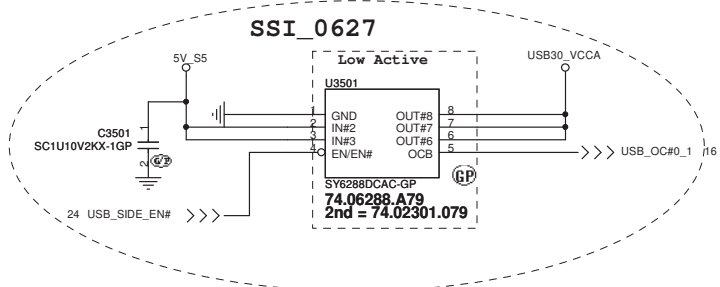
SSID = USB



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USB Power SW (U3501 & U3503)

Vendor	Vendor P/N	Wistron P/N	Priority
Silergy	SY6288DCAC	74.06288.A79	1ST
DI (Diodes)	AP2301MPG-13	74.02301.079	2ND
			3RD



SSID = Reset.Suspend

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<Core Design>



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Title

S3 Reduction

Size
A4

Document Number

Round Rock 13.3" UMA

Rev

X00

Date: Friday, June 28, 2013

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(Blanking)
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<Core Design>



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Taipei Hsien 221, Taiwan, R.O.C.

Title

Reserved

Size
A4

Document Number

Rev

Round Rock 13.3" UMA00

Date: Friday, June 28, 2013

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<Core Design>



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Title

Reserved

Size
A

Document Number

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X00

Date: Friday, June 28, 2013

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SSID = OBFF

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<Core Design>



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Title

Reserved

Size
A4

Document Number

Round Rock 13.3" UMA

Rev

X00

Date: Friday, June 28, 2013

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<Core Design>



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Title

Reserved

Size
A

Document Number

Round Rock 13.3" UMA

Rev

X00

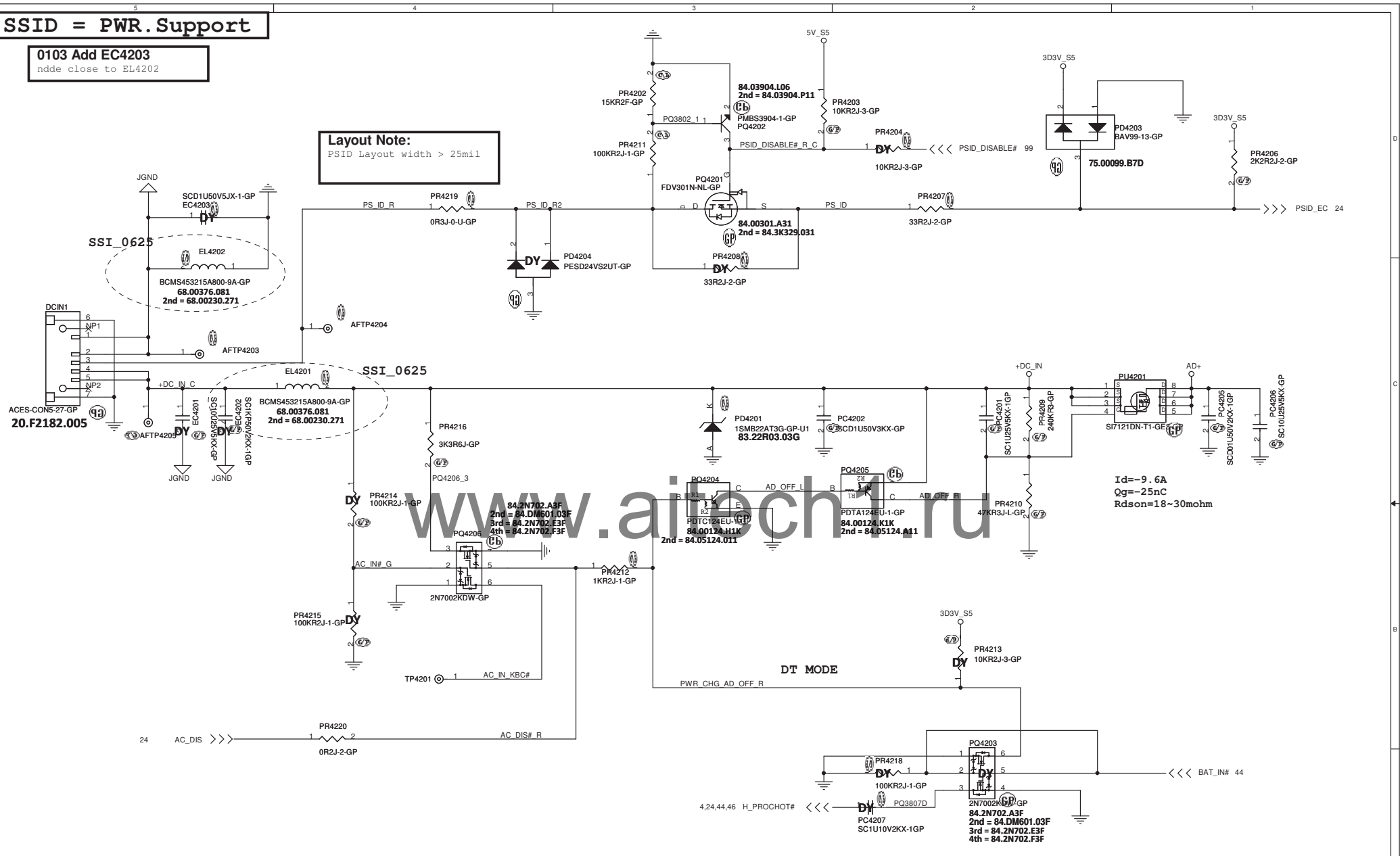
Date: Friday, June 28, 2013

Sheet 41 of 107

SSID = PWR.Support

0103 Add EC4203
ndde close to EL4202

Layout Note:
PSID Layout width > 25mil



<Core Design>

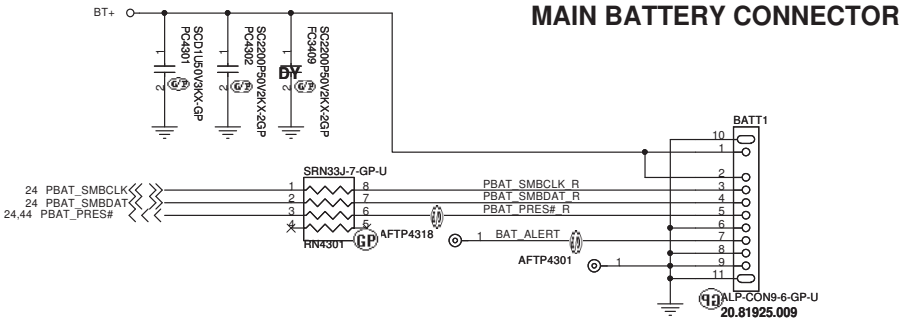
DELL Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: **DCIN JACK**

Size	Document Number	Rev
A3	Round Rock 13.3" UMA	X00

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SSID = PWR.Support



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BT-

PBAT_SMBCLK_R

PBAT_SMBDAT_R

PBAT_PRES#_R

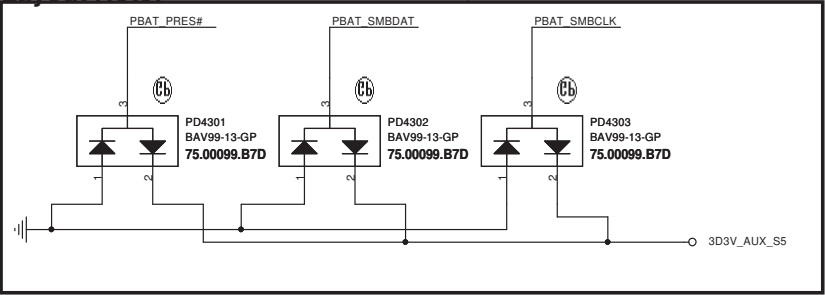
AFTP4302

AFTP4303

AFTP4304

AFTP4305

Layout Note: Place near Battery CONN



<Core Design>

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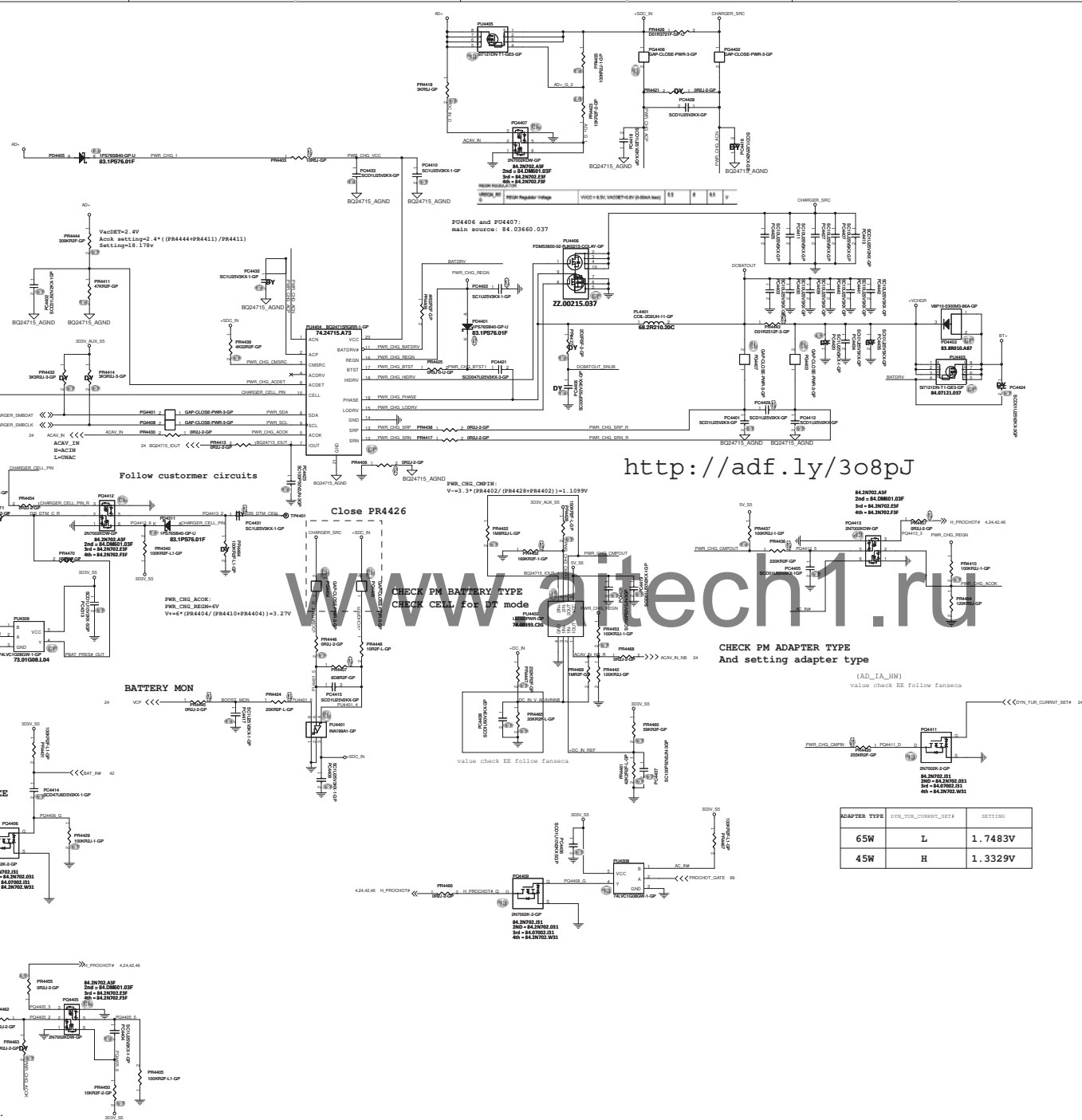
File

BATTERY CONN

Size A3 Document Number **Round Rock 13.3" UMA** Rev **X00**

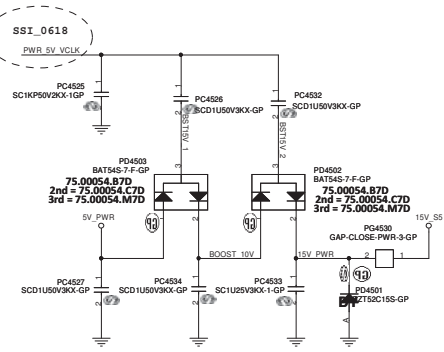
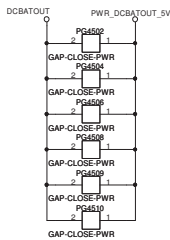
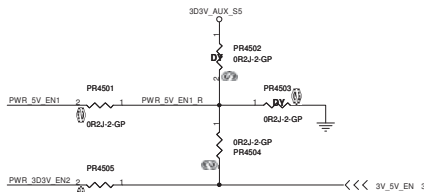
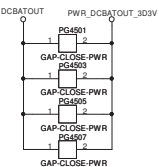
Date: Friday, June 28, 2013 Sheet 43 of 107

SSID = Charger

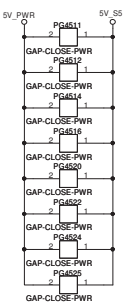
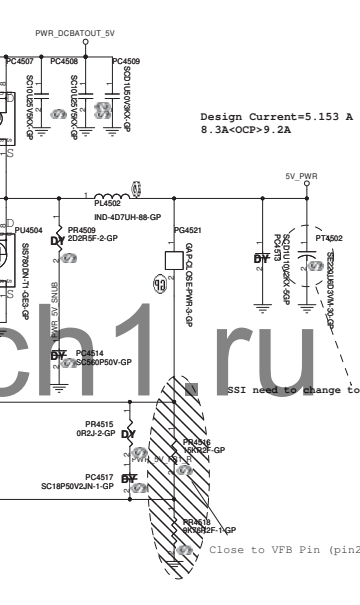
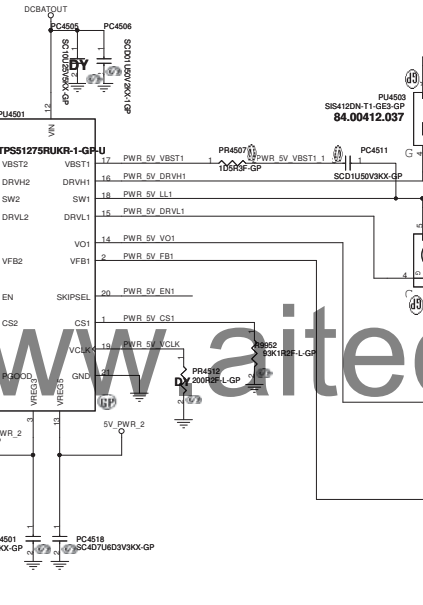
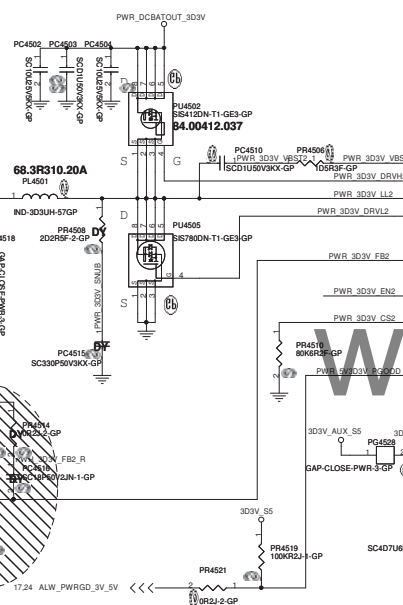
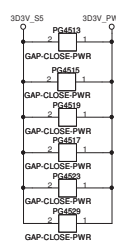


CHECK EE
follow customer circuits.

SSID = PWR.Plane.Regulator_5v3p3v



Design Current=5.894 A
8.841A<OCP>10.6A



SSI need to change to polymer cap

SSI need to change to polymer cap

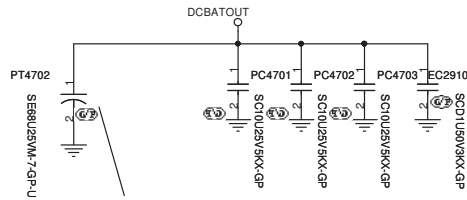
I/P cap: CHIP CAP C 10U 25V K0805 X5R/ 78.10622.51L
Inductor: CHIP IND 3.3UH PCMO063T-3R3MN Cyntec 28mohm/30mohm Isat =13.5Arms 68.3R310.20A
O/P cap: CHIP CAP POL 220U 6.3V M 6.3*4.5 /Matsuti/ 17mOhm / 77.52271.09L
H/S:SI5412DN-T1-GE3 / 24mOhm/30mOhm@4.5Vgs / 84.00412.037
L/S:SI5406DN-T1-GE3 / 11.5mOhm/14.5mOhm@4.5Vgs / 84.00406.037

I/P cap: CHIP CAP C 10U 25V K0805 X5R/ 78.10622.51L
Inductor: CHIP IND 3.3UH PCMO063T-3R3MN Cyntec 28mohm/30mohm Isat =13.5Arms 68.3R310.20A
O/P cap: CHIP CAP POL 220U 6.3V M 6.3*4.5 /Matsuti/ 17mOhm / 77.52271.09L
H/S:SI5412DN-T1-GE3 / 24mOhm/30mOhm@4.5Vgs / 84.00412.037
L/S:SI5406DN-T1-GE3 / 11.5mOhm/14.5mOhm@4.5Vgs / 84.00406.037

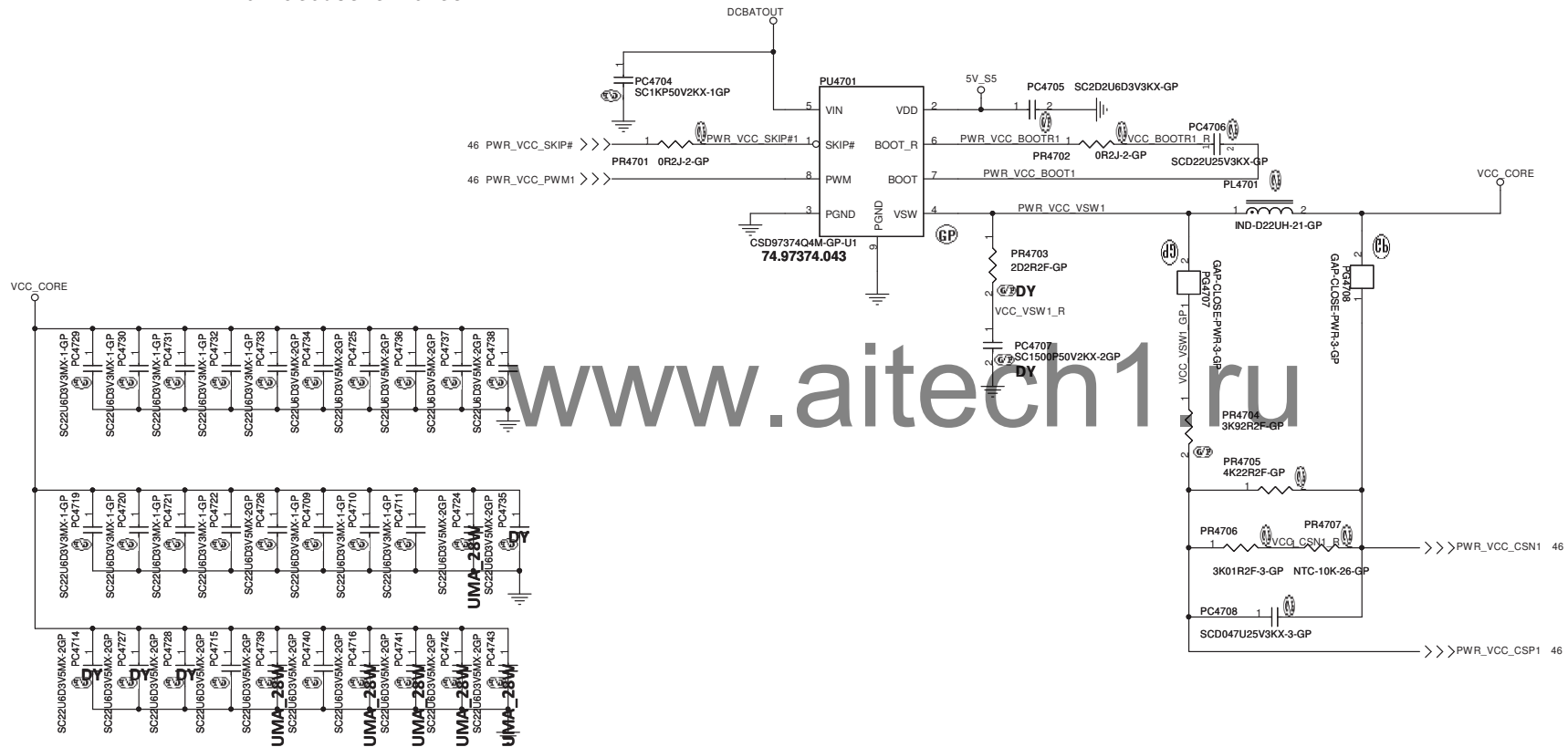
[illegible]

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
<i>TPS51622 CPUCORE(1/2)</i>			
Size A3	Document Number	<i>Round Rock 13.3" UMA</i>	Rev <i>X00</i>
Date:	Friday, June 28, 2013	Sheet	46 of 107

SSID = CPU.Regulator

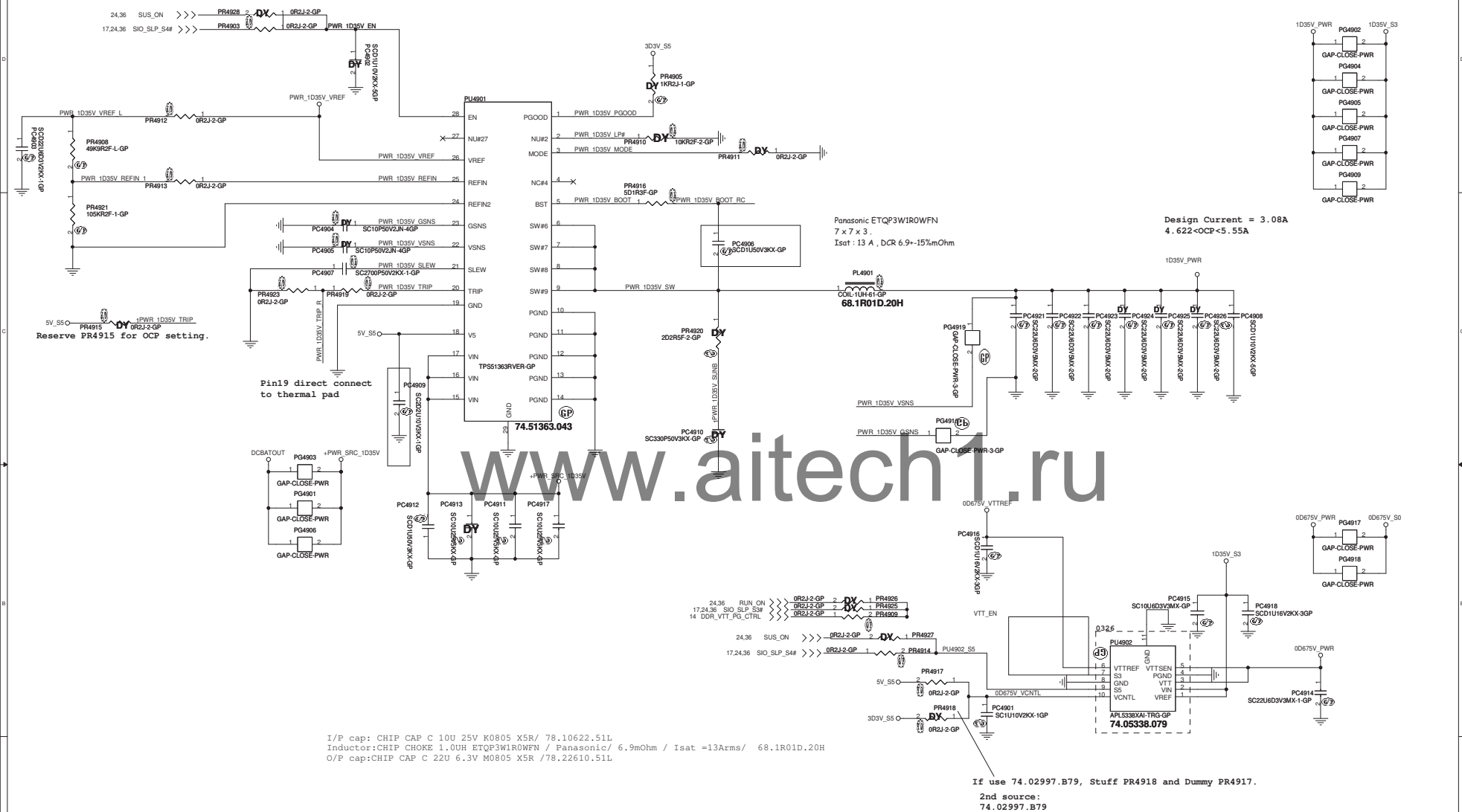


For acoustic noise



<Core Design>

SSID = PWR.Plane.Regulator lp35v0p675v



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Title

Reserved

Size
A4

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Date: Friday, June 28, 2013

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<Core Design>



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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Reserved

Size
A4

Document Number

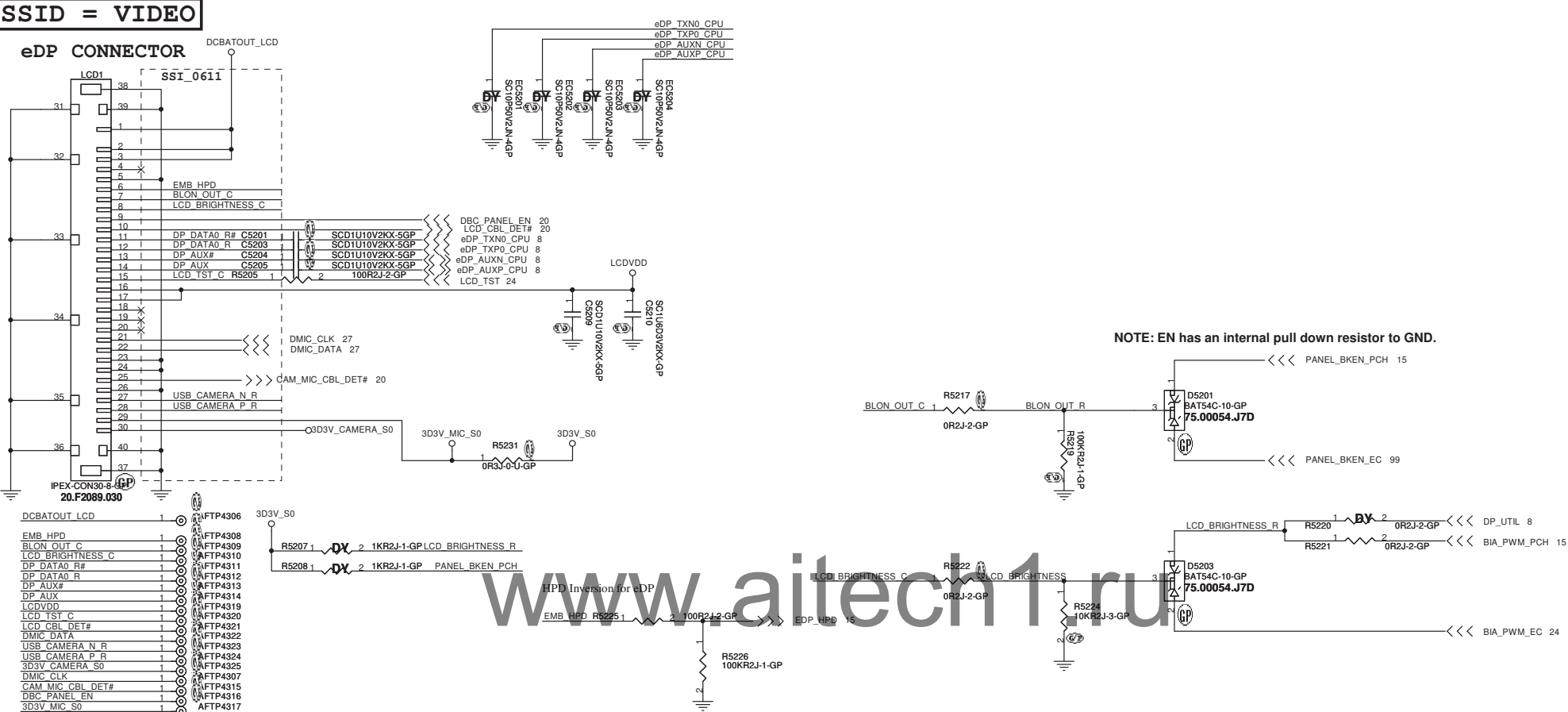
Round Rock 13.3" UMA

Rev
X00

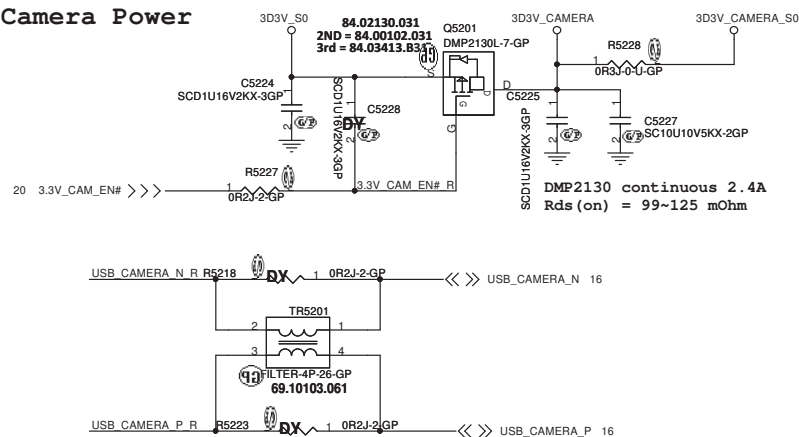
Date: Friday, June 28, 2013

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SSID = VIDEO

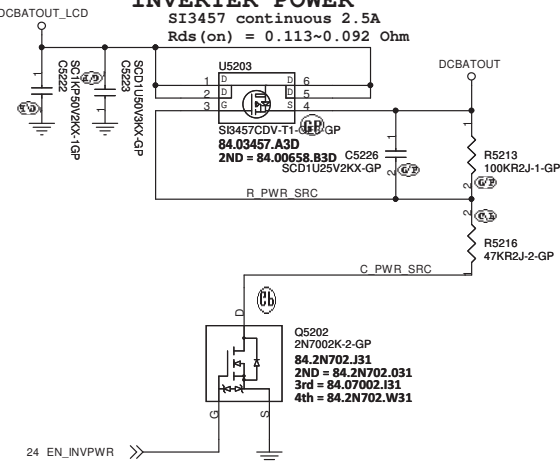


Camera Power



INVERTER POWER

SI3457 continuous 2.5A

$$R_{ds(on)} = 0.113 \sim 0.092 \text{ Ohm}$$


<Core Design>

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Title			
eDP Connector			
Size A3	Document Number		Rev
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<Core Design>



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Title

Reserved

Size
A4

Document Number

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Rev

X00

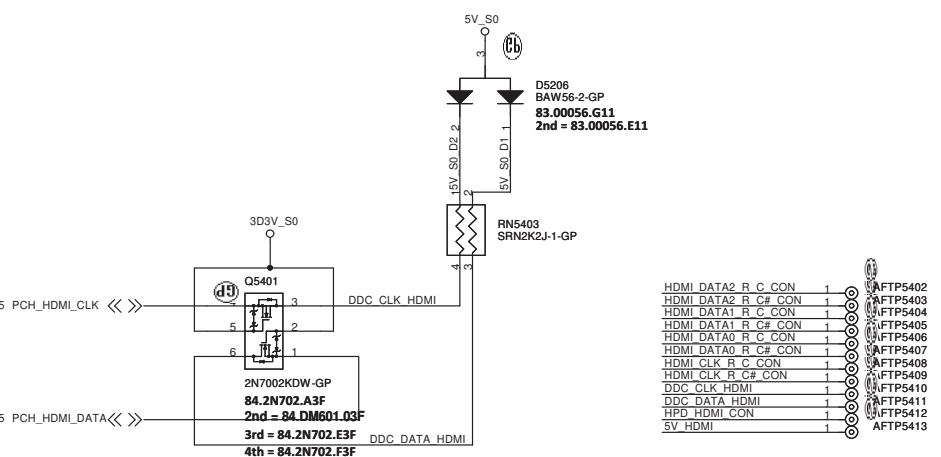
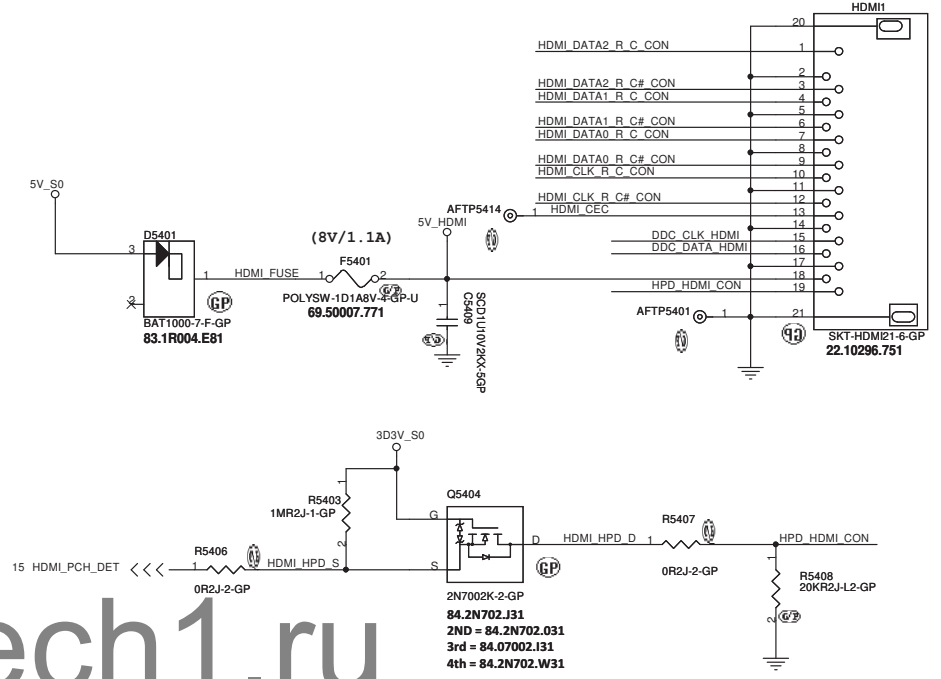
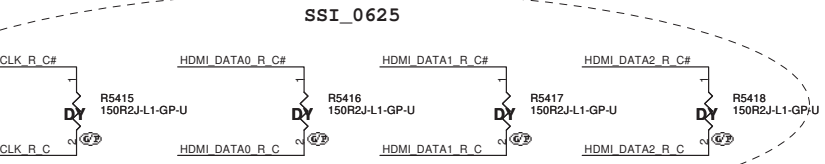
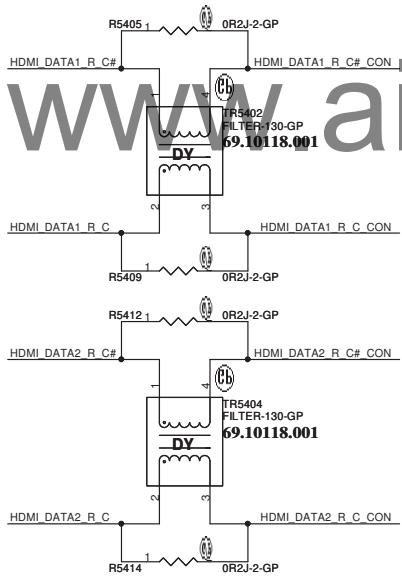
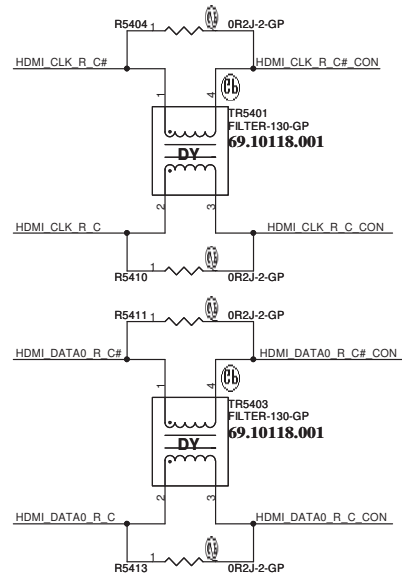
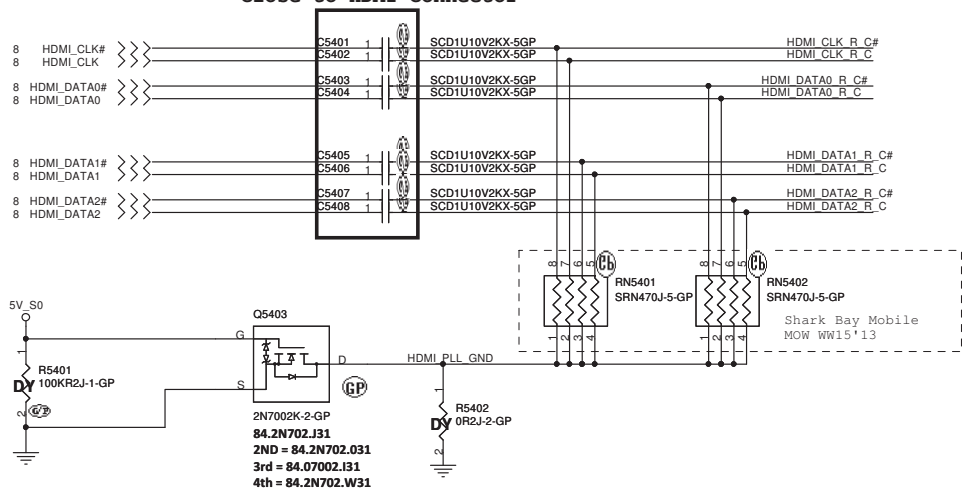
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SSID = VIDEO

HDMI CONNECTOR

Close to HDMI Connector



<Core Design>

DELL Wistron Corporation
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Title: **HDMI Level Shifter/Connector**

Size: A3 Document Number: **Round Rock 13.3" UMAX00**

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<Core Design>



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Title

Reserved

Size
A4

Document Number

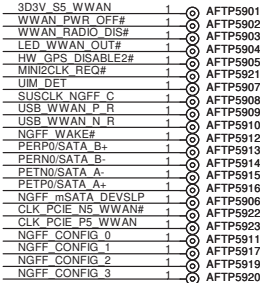
Round Rock 13.3" UMA

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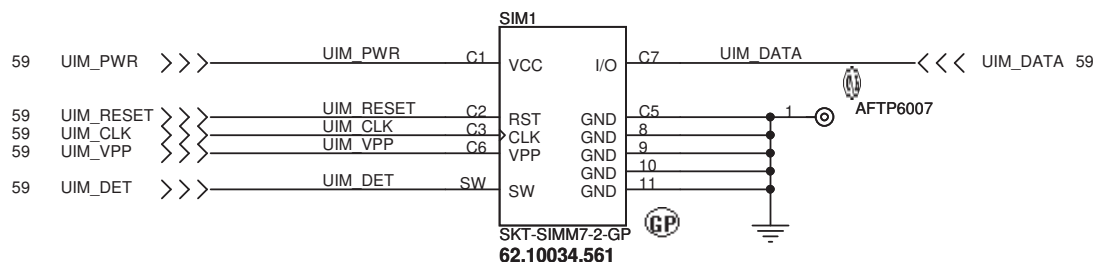
SSID = WIRELESS



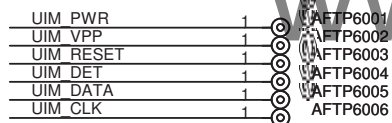
<Core Design>

	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
	Title		
Size	Document Number	NGFF-WWAN/SSD Round Rock 13" UMA	
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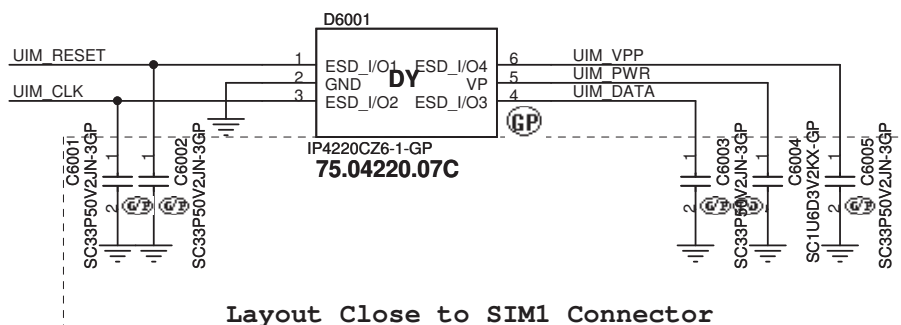
SSID =WIRELESS



PIN	62.10034.561 Micro SIM PinDefine
C1	VCC
C2	RST
C3	CLK
C4	Reserve
C5	GND
C6	VPP
C7	I/O
SW	SIM Card Detect
8	PTH GND
9	PTH GND
10	PTH GND
11	PTH GND



Change from 83.00005.BAE to 75.04220.07C



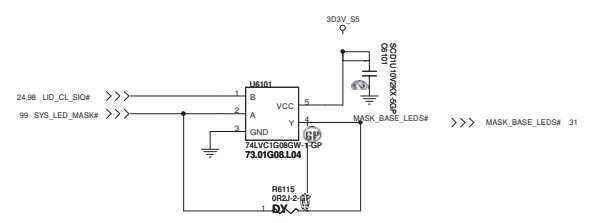
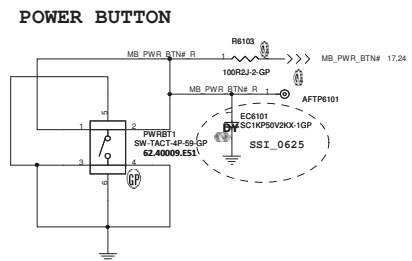
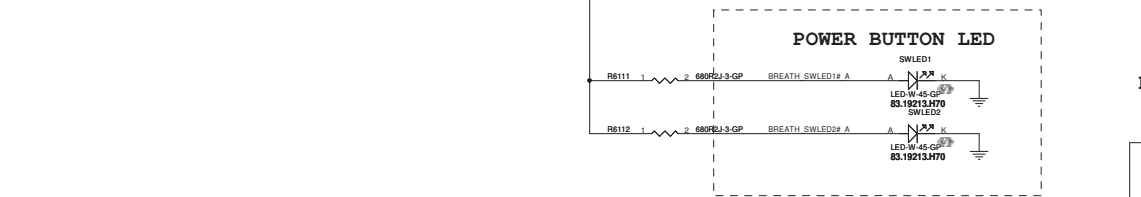
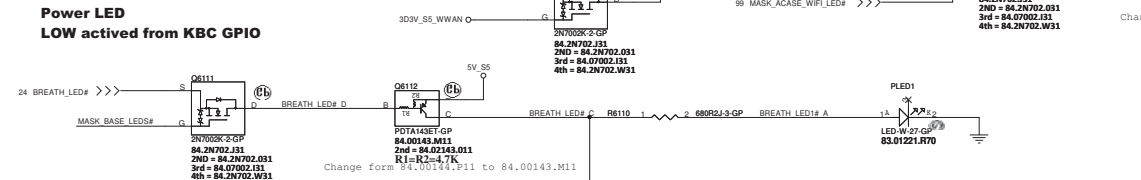
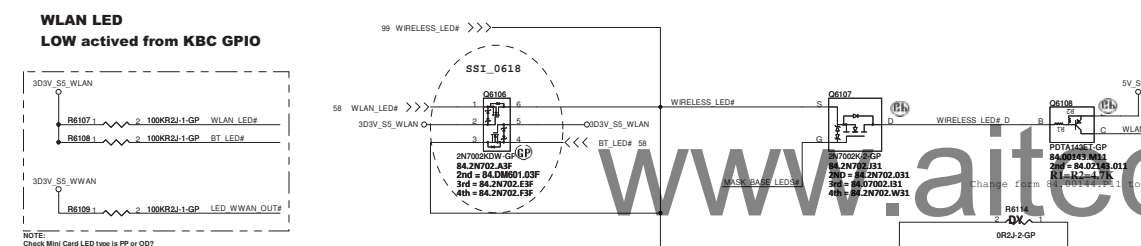
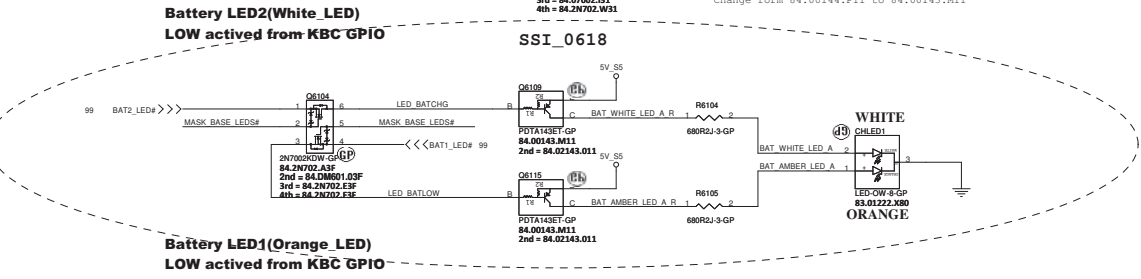
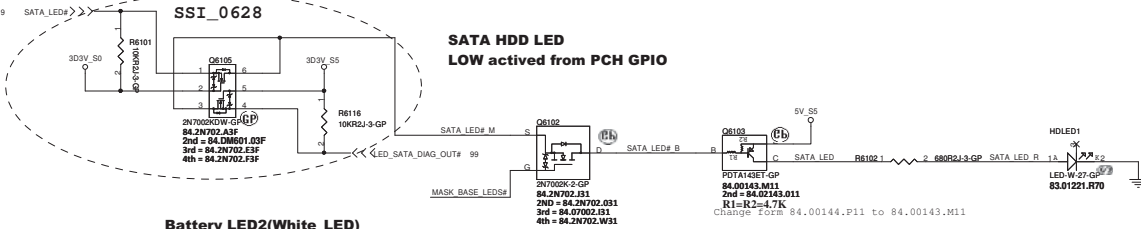
<Core Design>



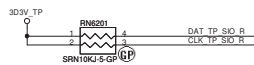
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Taipei Hsien 221, Taiwan, R.O.C.

Title		
mSATA		
Size	Document Number	Rev
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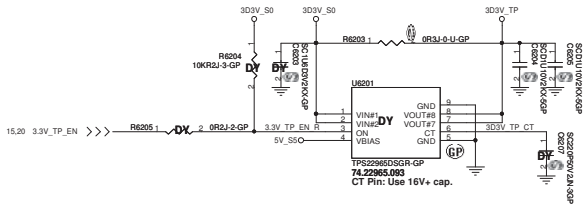
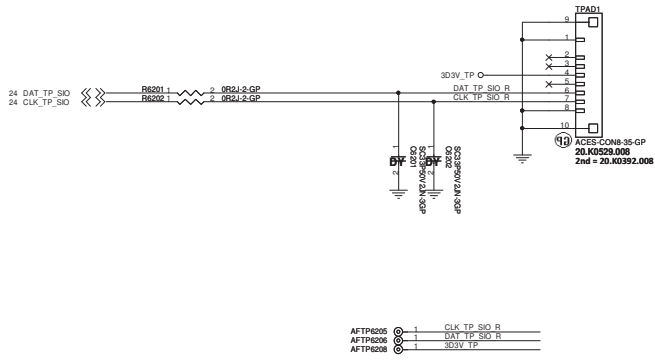
SSID = User.Interface



SSID = KBC SSID = Touch.Pad



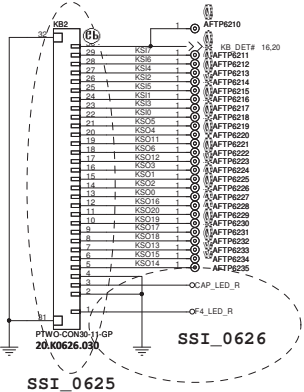
TouchPad Connector



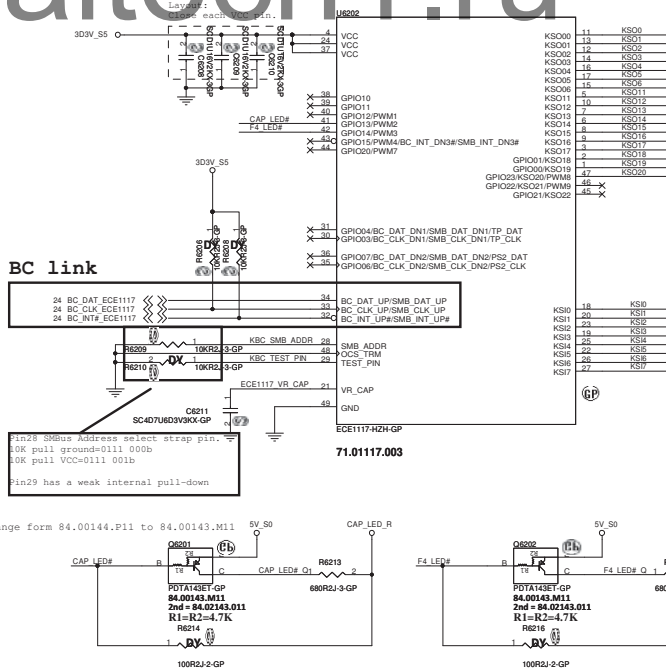
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KBC SMC ECE117

Internal KeyBoard Connector



MB Pin NO.	Description	Module Pin NO.
30	Diagnostic	1
29	KSI[7]:S8	2
28	KSI[6]:S7	3
27	KSI[4]:S5	4
26	KSI[2]:S3	5
25	KSI[5]:S6	6
24	KSI[1]:S2	7
23	KSI[3]:S4	8
22	KSI[0]:S1	9
21	KSO[5]:D6	10
20	KSO[4]:D5	11
19	KSO[11]:D8	12
18	KSO[6]:D7	13
17	KSO[12]:D9	14
16	KSO[3]:D4	15
15	KSO[1]:D2	16
14	KSO[2]:D3	17
13	KSO[0]:D1	18
12	KSO[16]:D13	19
11	KSO[20]:D17	20
10	KSO[19]:D16	21
9	KSO[17]:D14	22
8	KSO[18]:D15	23
7	KSO[13]:D10	24
6	KSO[15]:D12	25
5	KSO[14]:D11	26
4	GND	27
3	Caps Lock LED	28
2	GND	29
1	F4 LED	30



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IO CONN

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Title

Hall Sensor

Size

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Rev

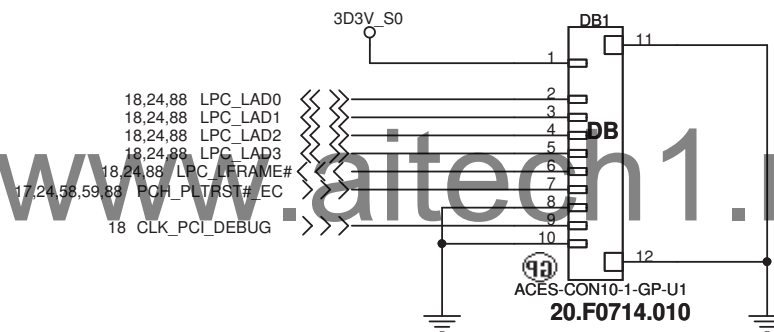
X00

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SSID = DEBUG PORT

SB modify to test pad



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Debug connector

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SENSOR

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Thunderbolt (1/5)

Size
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Title

Thunderbolt (2/5)

Size
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Title

Thunderbolt (3/5)

Size
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	5	4	3	2	1
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	5	4	3	2	1

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<Core Design>

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title <i>Thunderbolt (4/5)</i>			
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Title

Thunderbolt (5/5)

Size
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	5	4	3	2	1
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	5	4	3	2	1

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		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
<i>GPU (1/5) PEG</i>			
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Title

GPU (2/5) DIGITAL

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Title

GPU (3/5) VRAM

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Title

GPU (4/5) GPIO

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Title

GPU (5/5) PWR/GND

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Title

VRAM1,2 (1/4)

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Title

VRAM3,4 (2/4)

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Title

VRAM5,6 (3/4)

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Title

VRAM7,8 (4/4)

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	5	4	3	2	1
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	5	4	3	2	1

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		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
<i>VGA CORE</i>			
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	5	4	3	2	1
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	5	4	3	2	1

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<Core Design>

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
		Title DISCRETE VGAPOWER	
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<Core Design>



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Title

Switchable GFXLCD

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Title

Switchable GFXCRT

Size
A

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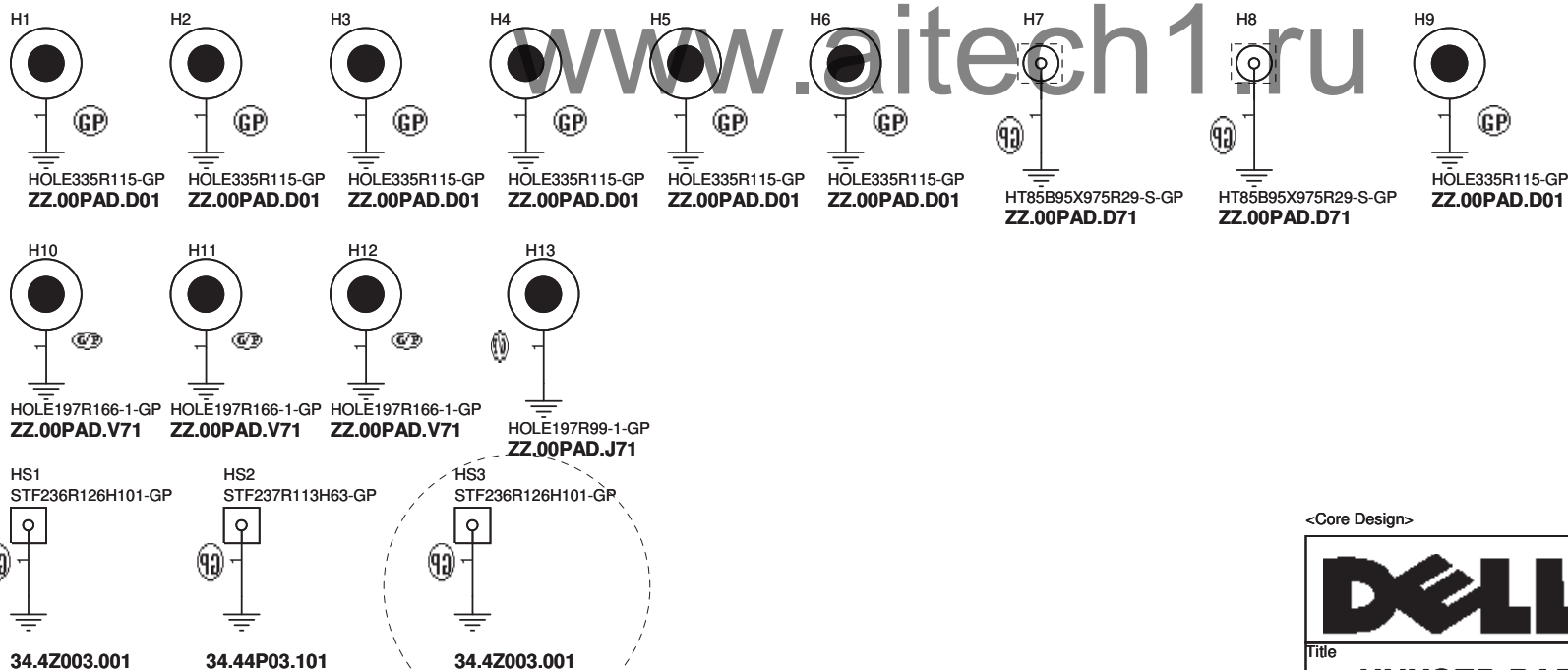
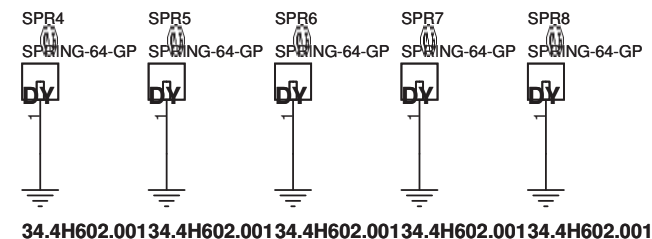
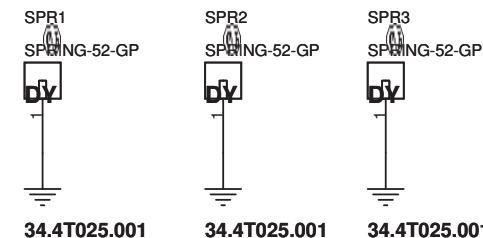
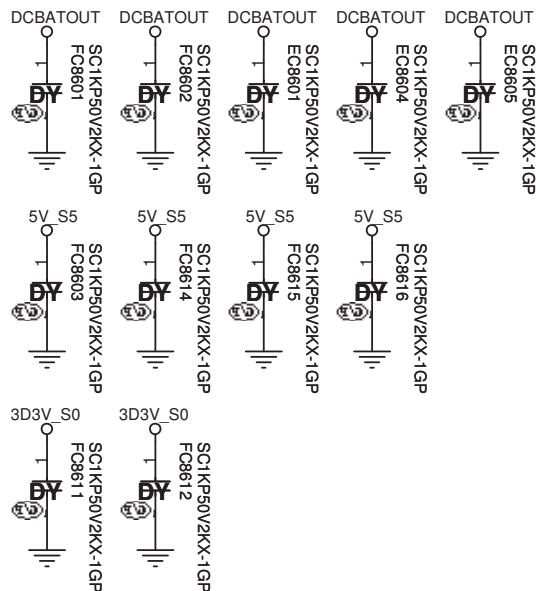
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Title

UNUSED PARTS/EMI Capacitors

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SSID = USH

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Title

USH Board Connector

Size
A4

Document Number

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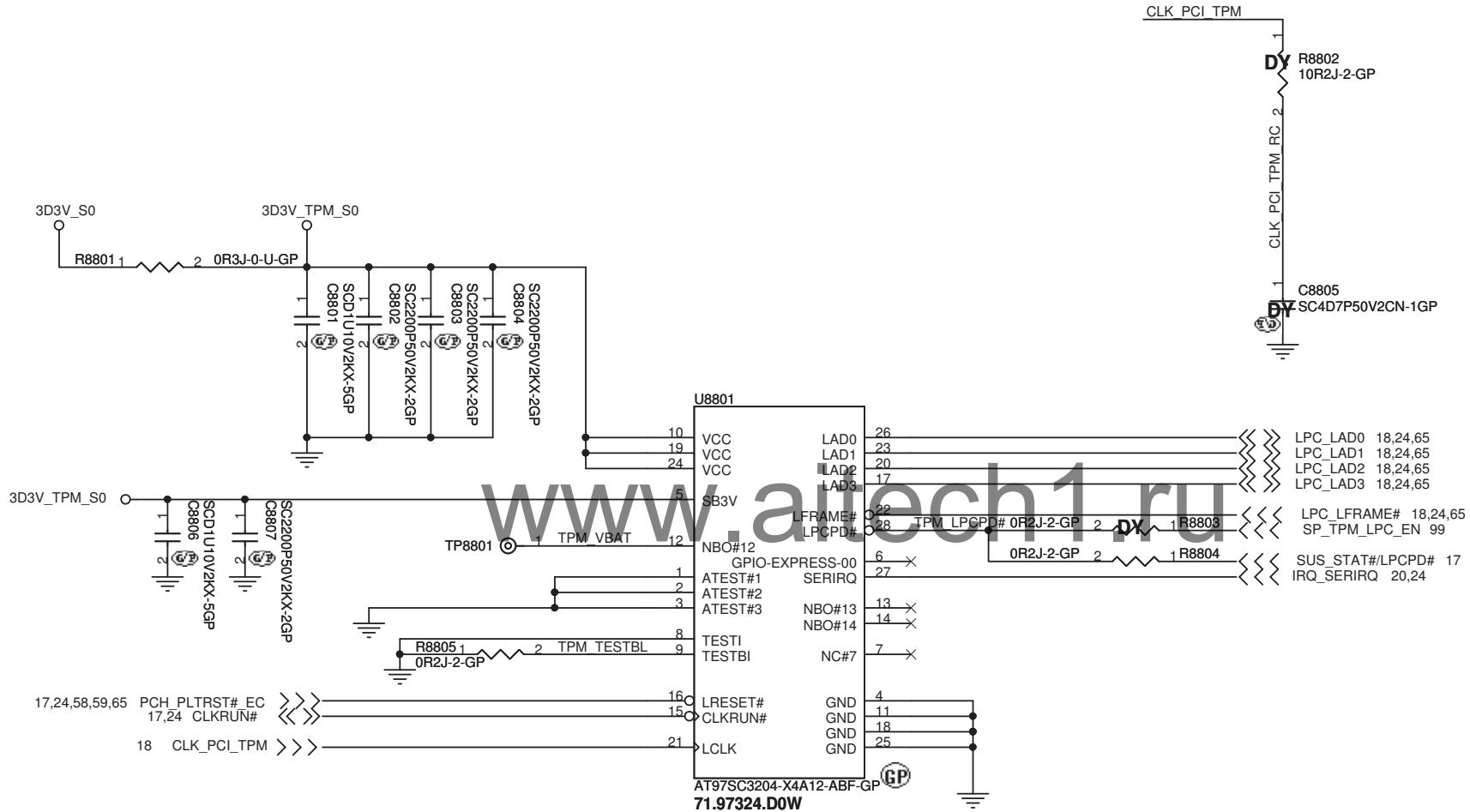
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SSID = TPM

Place close to Pin 21



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Title

TPM

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Title

Finger Print

Size
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Title

NFC Connector

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Title

Smart Card

Size

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<Core Design>

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SSID = Docking

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Title

DOCKING

Size
A4

Document Number

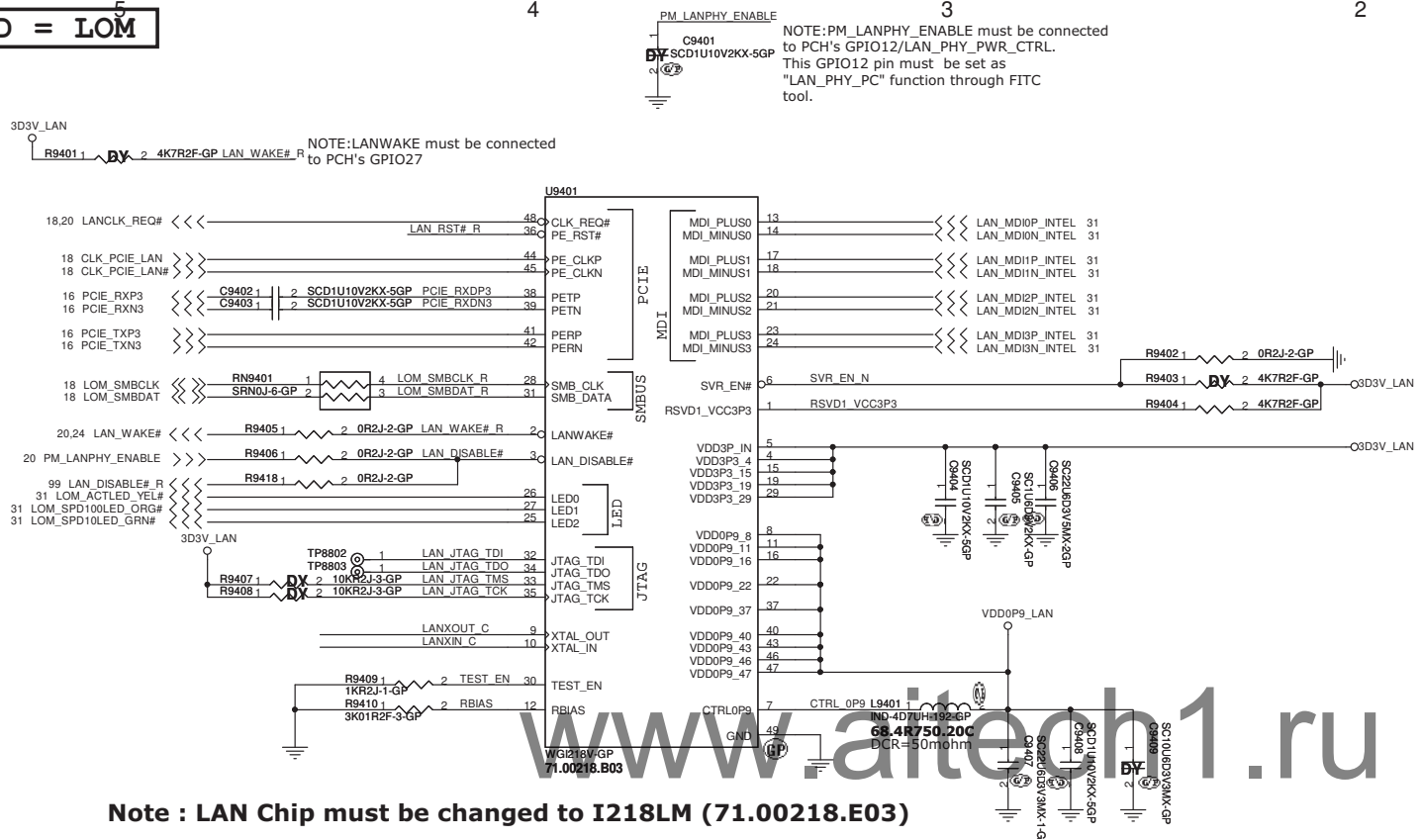
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SSID = LOM

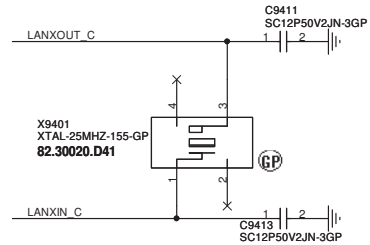
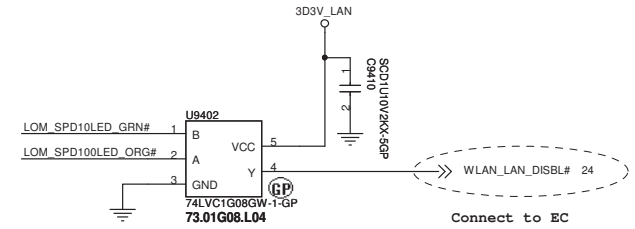
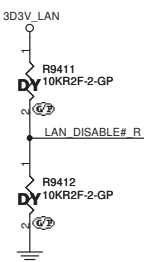


0D9V Power Options
SVR_EN_N: Pull High External
Pull Low Internal

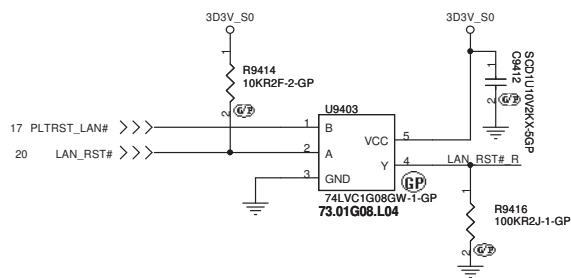
Internal SVR	Shared with external 1.05V SVR
L9401: STUFF	L9401: NO STUFF
R9413: NO STUFF	R9413: STUFF
R9402: STUFF	R9402: NO STUFF
R9403: NO STUFF	R9403: STUFF

*NOTE: Clarkville has 0.9V internal SVR. However it is also possible to disable this 0.9V iSVR and Clarkville can support the external 1.05V supply. When sharing, make sure the 1.05V_LAN is controlled by the SLP_LAN signal.

Note : LAN Chip must be changed to I218LM (71.00218.E03)



NOTE: In most designs Cstray= \sim 6 pF, so C7=C8 should be \sim 24 pF as a good starting point for a Cload=18 pF crystal. If 24 pF cap is not available, 22 pF or 27 pF value can be used as a starting point. Value will vary depending on the specific board layout stackup and which crystal part is used. Each design should check crystal's ppm to make sure it is within the Clarkville specification



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LAN SW

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A4

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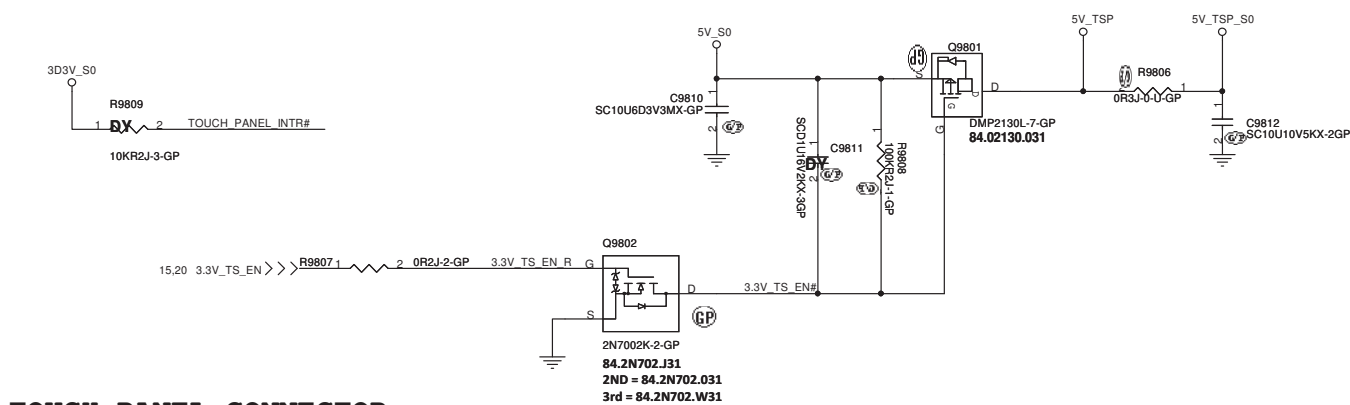
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SSID = User.Interface

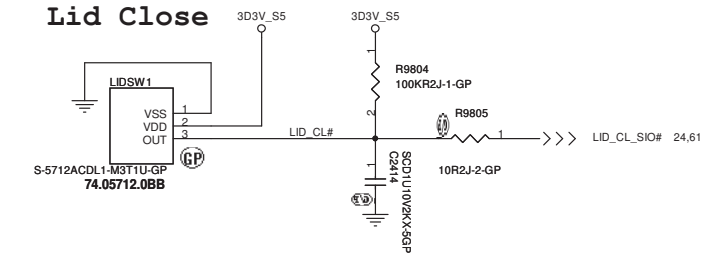
TOUCH PANEL POWER



TOUCH PANEL CONNECTOR

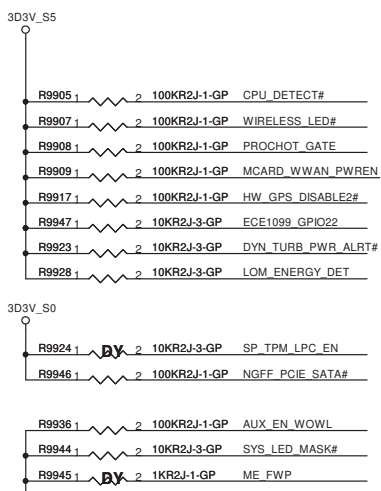
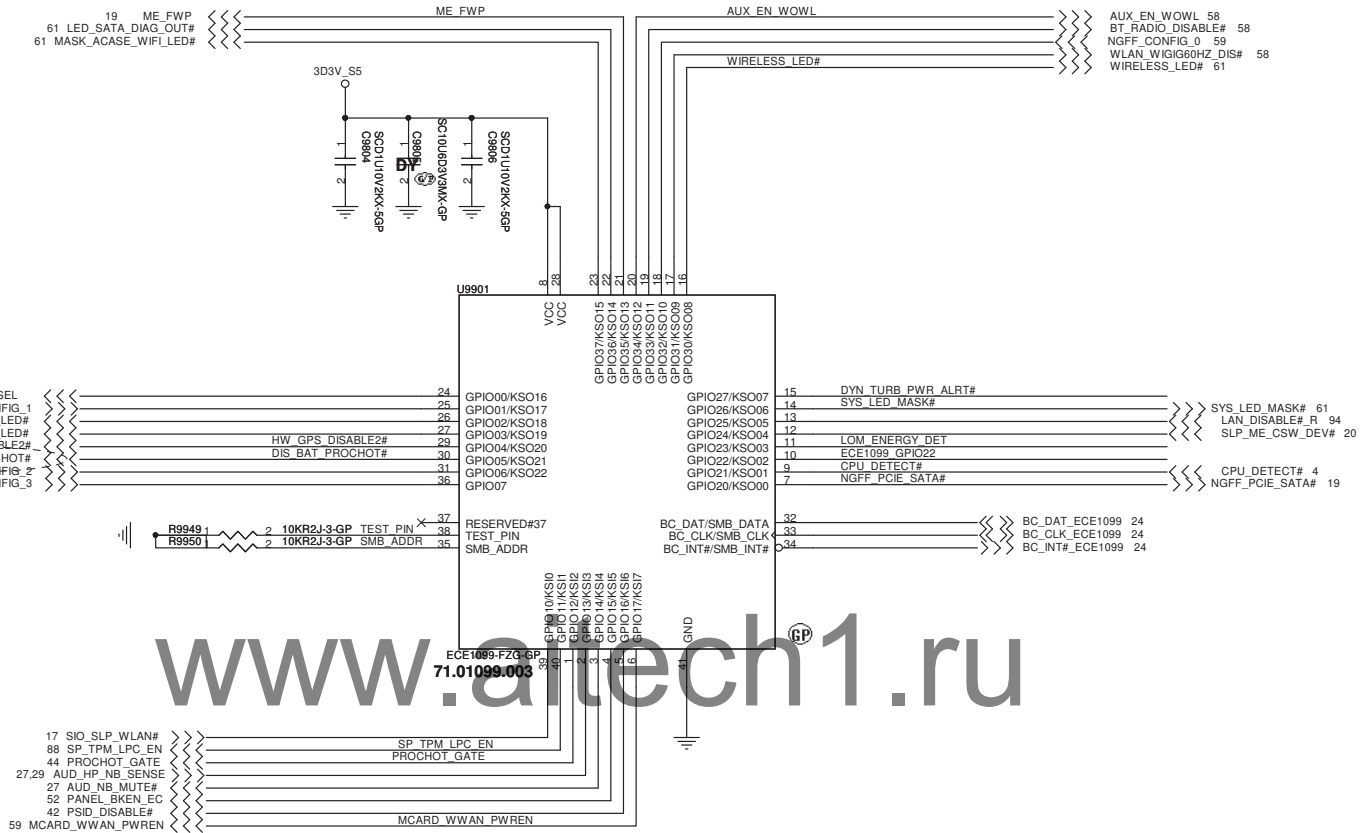


Lid Close



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SSID = SIO



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